Polymer-Based Wafer-Level Packaging of Micromachined HARPSS Devices

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Polymer-Based Wafer-Level Packaging of Micromachined HARPSS Devices

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DEDICATION

To my loved parents

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SUMMARY

This thesis reports on a new low-cost wafer-level packaging technology for microelectromechanical systems (MEMS). The MEMS process is based on a revised version of High Aspect Ratio Polysilicon and Single Crystal Silicon (HARPSS) technology. The packaging technique is based on thermal decomposition of a sacrificial polymer through a polymer overcoat followed by metal coating to create resizable MEMS packages. The sacrificial polymer is created on top of the active component including beams, seismic mass, and electrodes by photodefining, dispensing, etching, or molding. The low loss polymer overcoat is patterned by photodefinition to provide access to the bond pads (or probing pads). The sacrificial polymer decomposes at temperatures around 200-280°C and the volatile products permeate through the overcoat polymer leaving an embedded air-cavity. For MEMS devices that do not need hermetic packaging, the encapsulated device can then be handled and packaged like an integrated circuit. For devices that are sensitive to humidity or need vacuum environment, hermeticity is obtained by deposition and patterning thin-film metals such as aluminum, chromium, copper, or gold.

To demonstrate the potential of this technology, different types of capacitive MEMS devices have been designed, fabricated, packaged, and characterized. This includes beam resonators, RF tunable capacitors, accelerometers, and gyroscopes. The MEMS design includes mechanical, thermal, and electromagnetic analysis to obtain a thorough understanding of the MEMS and the associated packaging. The device performance,

before and after packaging is compared and the correlation to the model is presented. In the process of this work, new fabrication techniques are explored and reported.

Many MEMS packaging methods are reported for only a special device. The main packaging methods include wafer-to-cap bonding and sacrificial-layer-based sealing. The wafer bonding schemes are the most reliable methods, but are costly and not size efficient. The sacrificial-layer-based sealing schemes are device-dependent, costly, and mainly high-temperature. These methods require perforation in the package to release the sacrificial film, followed by multiple steps to seal the holes. The elevated temperature during packaging sequence introduces stress on the MEMS device and can degrade the performance. The advantages of the presented approach compared to other MEMS packaging techniques are that it is a low-temperature process that can be used for packaging a wide variety of MEMS including metallic structures, it produces a low-profile encapsulating cover, and can be performed on any substrate. Thermal decomposition of sacrificial polymer is performed through a solid perforation-free capsule, which eliminates the steps needed in some other sacrificial-film-based techniques to seal a perforated or porous cover. It does not require high temperature deposition and etching of sacrificial materials and is stiction-free. The overcoat geometry can be scaled as needed by the application to tailor different sizes from microscale to millimeter-scale. The packaging does not require wafer-to-cap alignment and bonding. This method does not impose any limitation on MEMS size, topology, or substrate. New MEMS and package characterization methods including evaluation of the package permeability, stress, and cavity pressure are presented.

The following is a summary of the main contributions of this work to the extensive research focused on MEMS systems and their packaging technologies:

1) A new *low-cost wafer-level packaging method* for bulk or surface micromachined devices including resonators, RF passives and mechanical sensors is reported. This technique utilizes thermal decomposition of a sacrificial polymer through an overcoat polymer to create buried cavities on top of the resonant/movable parts of the micromachined device. It provides small interconnections together with resizable package dimensions. We report MEMS package thicknesses in the range of 10 μm to 1 mm, and package size from 0.0001 mm^2 to 1 mm^2.
2) A revised version of the HARPSS technology is presented to implement *high aspect ratio silicon capacitors, resonators and inertial sensors* in the smallest area.

CHAPTER I

INTRODUCTION AND BACKGROUND

Wafer-level packaging represents a challenging and costly task in the manufacturing of microelectromechanical systems (MEMS) [1, 2]. On average, 60-90% of the cost of a MEMS device is in the package. The package protects the MEMS device against detrimental effects of the environment such as moisture and dust. A hermetic package is required for the MEMS devices operating in vacuum such as resonators and gyroscopes. The package provides design-specific functions, such as mechanical stability and radiation protection required for sensors and RF signal isolation for RF passives. The lifetime and noise performance of high-quality MEMS accelerometers and gyroscopes used in space gravity instruments can be enhanced by using proper packaging. Wideband packaging is required to seal RF MEMS components including switches and variable capacitors (varactor). A micromechanical switch can fail because of humidity, and imposes more restrictions on the hermeticity of the package, compared to MEMS varactors.

The main reason for moving from chip-scale to wafer-level packaging is the cost. Moreover, since wafer-scale packaging is done prior to assembly, there will be less chance of damaging the MEMS during the high temperature molding process.

The most simple example of wafer-scale packaging is the addition of a protective microshell over the active MEMS component that can provide the required sealing for further packaging, handling and assembly with leadframes.

This dissertation introduces, for the first time, the development of a low-cost and low temperature packaging technique, suitable for any type of MEMS device. The Wafer-Level Metal-Organic Package (WLMOP) for different varieties of MEMS is designed and implemented to demonstrate the strength of the technology. The thesis is organized in five chapters. A brief outline of the dissertation is presented below.

Chapter 1 introduces the motivation behind the research work and the background. This chapter gives a general overview and history of wafer-level packaging of micromachined devices. Also discussed in this chapter are the MEMS accelerometers and variable capacitors, as candidates for microscale and mesoscale packaging.

Chapter 2 introduces microgravity silicon accelerometers. The sensors are realized through the High Aspect-Ratio Single-Crystal Silicon and Polysilicon (HARPSS) process. The physics of the squeeze film damping in the inertial sensors is discussed and methods for decreasing the sensor total noise are demonstrated. The chapter covers the design, thermal, mechanical and electrostatic analysis, fabrication, and sensitivity characterization of HARPSS accelerometers in silicon and silicon-on-insulator substrates. Major challenges including polysilicon etching, oxidation-induced beam buckling, and micron-scale corrugation are outlined.

Chapter 3 introduces low-profile low-voltage silicon varactors. The fabrication is an advanced single crystal silicon HARPSS process, which uses gold evaporation to increase the electrical quality factor. The varactor modeling includes mechanical and three-

dimensional electromagnetic analysis before and after packaging. The chapter includes design, fabrication, and DC and RF characterization of different types of varactors.

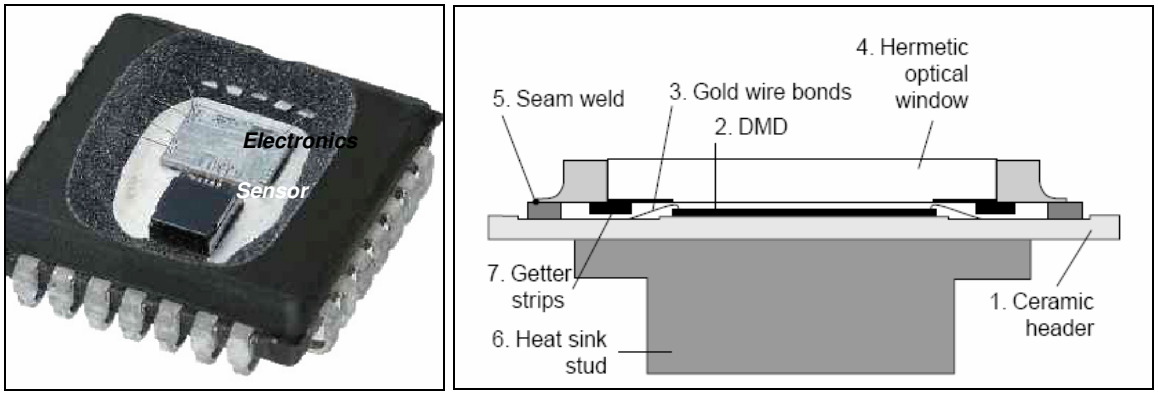
Chapter 4 presents the generic wafer-level packaging sequence flow and implementation of the packaging on beam resonators, varactors, and inertial sensors. A comparison of the performance of devices before and after packaging is given. Also discussed in this chapter is the measurement of the polymer package gas permeability and evaluation of cavity pressure. Electro-mechanical analysis of the package is provided to verify the experiments. A thorough study of how the residues degrade the Q factor of packaged resonators is presented. The packaging parameters are optimized to minimize the amount of residues without sacrificing the overcoat integrity.

Chapter 5 the thesis ends with a conclusion of the information presented, and also suggests the future directions and thoughts on extending the present body of work.

1.1. Review of Wafer-Level MEMS Packaging Technologies

Most MEMS inertial sensors are fabricated using techniques that leave the mechanical structures exposed after wafer fabrication is completed. Open-die MEMS devices are easily destroyed if their unprotected mechanical elements come in contact with a physical object; they are also very susceptible to degradation by dust, stiction, and corrosion by water vapor. For instance, RF micromechanical switches do not survive a normal lab environment and will collapse as a result of humidity-induced stiction. To ensure long-term reliability, an open-die MEMS device must be hermetically packaged. Packaging is normally the most expensive part of microsystem manufacturing. There are two general solutions to MEMS packaging. One approach is to use the existing IC

infrastructure, chip-scale ceramic packaging, where release and sealing are performed serially on the individual die after dicing. Figure 1.1.a shows a chip-scale packaged accelerometer and interface circuit from Bosch. Figure 1.1.b shows a packaged Digital Micromirror Device (DMD) from Texas Instruments [3]. The DMD is adhesively attached to the Al_2O_3 ceramic header and then wire bonded. The optical window is assembled to the ceramic header seal ring. The ceramics have Coefficient of Thermal Expansion (CTE) in the range of 5-9 ppm/°C, which is close to silicon (2.6 ppm/°C). CTE mismatch is more critical when the die size is larger. Because ceramic shrinks during the firing process, the package should be compensated in the design. The challenge in chip-scale packaging is selecting the specific equipments required to seal a die. Handling MEMS chips or dies prior to packaging is costly and inefficient from a manufacturing standpoint.



(a) (b)

Figure 1.1. a) Chip-scale packaged MEMS accelerometer system from Bosch RTC, b) Chip-scale packaged digital micromirror (DMD) from Texas Instruments [3].

The other approach is wafer-scale packaging, in which release and sealing are performed in parallel prior to dicing and assembly. Sealing the dies simultaneously on the wafer level, results in a reduction in size, time, and cost. Wafer-level packaging can be

classified into wafer-to-cap bonding and sacrificial-film-based sealing techniques. Wafer bonding is typically done by bonding a cap with a cavity onto the MEMS wafer [8-32]. Thin-film sealing can be done by surface micromachining to create a thin-film overcoat on top of a sacrificial material, followed by sacrificial film removal. Both techniques are discussed in sections 1.1.1 and 1.1.2.

1.1.1. Wafer-Bonding Techniques

Wafer bonding can be classified according to the cap material, the sealing material, or the feedthrough. Wafer capping includes direct bonding (anodic and fusion bonding), and bonding using intermediate layers. The latter method includes metals (solder [4], eutectic [5], Thermo-Compression Bonding (TCB) [10]), or insulators [13] (reflowed glass frit bonding [11], or adhesive bonding [12]). A summary of bonding methods for MEMS packaging is given in Table 1.1.

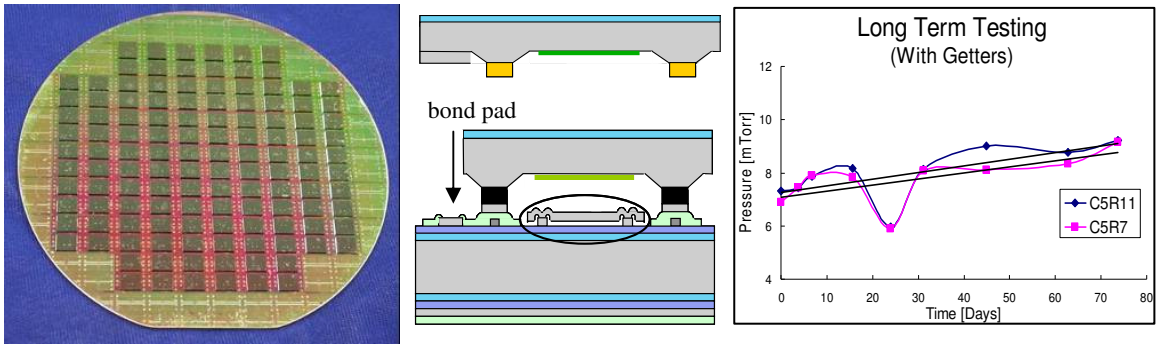
Table 1.1. Bonding techniques for MEMS packaging.

Bonding method			Material	Temperature	Comments
Direct Bonding		Anodic (electrostatic)	Glass to Si/glass/metal [7,8]	180-500°C	High voltage, surface roughness~1 μm hermetic
		Fusion (direct)	Si to Si/SiO_2 [9]	> 800°C	surface roughness ~ 4 nm, hermetic
Intermediate Bonding	Metal	Eutectic	Thin Au to Si [4]	363°C	Non-uniform, needs smooth surface, hermetic
		Solder	Au-Sn or Pb-Sn to Si [3]	183°C	Non-uniform, needs smooth surface, hermetic
		TCB	Thick Au to Si [10]	25-250°C	Hermetic
	Insulator	Adhesive	SU-8, BCB, polymide [12]	< 300°C	Not hermetic
		Melting	Reflowed glass frit: Si to Pyrex [11]	375-410°C	hermetic

Fusion bonding happens due to chemical reaction between OH-bonds of the hydrophilic surface [18]. High temperature annealing is required for increased bond strength that limits its usage for MEMS packaging. Moreover, it needs extra smooth

surfaces. Anodic bonding utilizes sodium-rich glass (e.g. Corning Pyrex 7740 or 8329) to pull the ultra flat silicon and glass into intimate contact by electrostatic force (0.2-1 kV). Glass is a biocompatible material and has a CTE (2.8 ppm/°C for Pyrex 8329) close to silicon (2.6 ppm/°C). Anodic bonding requires a surface roughness of better than 1 µm. Moreover, the sodium contamination during anodic bonding can cause significant change to CMOS-based MEMS systems, such as shifting the threshold voltage.

Bonding using intermediate layers (metals or insulators) can be performed at much lower temperatures. Metallic bonding methods can seal to rough surfaces at low temperatures. The alloy composition is selected to minimize the melting point. The large CTE mismatch between metal (14.2 ppm/°C for Au-Si and 24.7 ppm/°C for Pb-Sn) and silicon is an issue that limits the thermal range of operation. The eutectic bonding reported in [5] is shown in Figure 1.2. Figure 1.2.a shows the fully packaged wafer. The eutectic bonding method starts with deposition and patterning of gold on the cap wafer, followed by etching the cavity on wafer (Fig. 1.2.b). After depositing getters to the cap wafer, it is aligned and bonded to the MEMS wafer. (Fig.1.2.c). Above 363°C, the polysilicon on the bond rings diffuses into gold to form the eutectic bond.



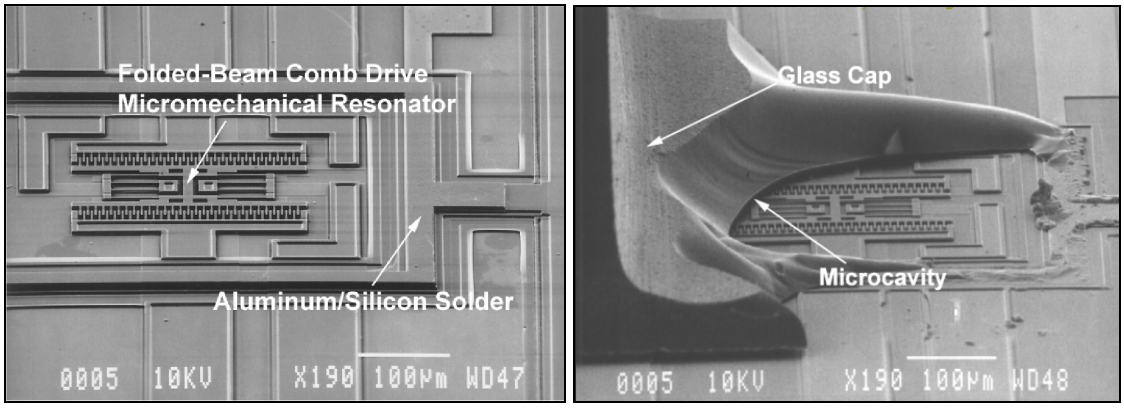
(a) (b): top, (c): bottom (d)

Figure 1.2. Process flow for the Eutectic bonding :a) Wafer with 132 vacuum packaged devices, b,c) Process flow: (b) After 2.5 µm gold deposition, patterning, bulk etching of the cavity, and getter deposition, c) After bonding, d): vacuum package results [5].

Fig. 1.2.d shows test results using a Pirani gauge, based on heat transfer from a suspended heater to a heat sink through a gas, where the gas thermal conductivity changes with package pressure. A base pressure of 6.9 mTorr and a leak rate of 8.5 mTorr/year are reported. Bonding using insulators include patterning adhesives, melting the intermediate layer, forming a stable intermediate compound (diffusion), or heating up to 50-70% of melting point of the intermediate layer (brazing). The adhesives include polymer, epoxies, or UV-photoresists such as SU-8 [12], Benzocyclobutene (BCB) [13], polymides, and AZ4000. The adhesive is generally screen printed, and can be cured at room temperature or may require UV exposure for glass wafers or a thermal cure at 80 to 150°C. Reflow glass sealing is another technique that has been used for more than two decades to fabricate pressure sensors, accelerometers, gyroscopes and switches to join two silicon wafers together. Frit-glass is a mixture of lead borate or solder glass into a paste, which can be patterned onto a wafer using a silk-screen technique. Upon heating, it reflows and becomes glassy, and can glue two wafers. Reflowed glass frit sealing has traditionally been used in [10] with a dielectric seal that can conformally cover minor surface steps and even particles. In all intermediate bonding methods, bonding can be done at low temperatures and for rough surfaces without causing large thermal mismatch. But hermeticity is a consideration, because of outgassing of the polymers or epoxies used in the interface.

To avoid high-temperature bonding, all the mentioned bonding methods can be performed locally, by concentrating the bond energy to a small ring around the active area to avoid the thermal-sensitive MEMS to be affected [15]. Local bonding can be done by localized Chemical Vapor Deposition (CVD) bonding [16], RF dielectric heating [17],

localized ultrasonic bonding, local fusion bonding [18], local eutectic/solder bonding by running current through microheaters [19], or by CO_2 laser welding [20]. A classical example of local solder bonding is shown in Figure 1.3 for a vacuum packaged resonator. Polysilicon is deposited by Low Pressure CVD (LPCVD) to form the microheaters. The intermediate layer used for bonding is indium solder and the local bonding temperature is around 700°C. The strong bond is due to formation of silicon precipitate and aluminum oxide to provide a huge bonding strength. Accessing the MEMS contacts is achieved by horizontal aluminum feedthroughs at the surface. Additionally, bonding of aluminum to glass or silicon nitride can be performed using Rapid Thermal Processing (RTP) to elevated temperature at around 750°C for a small duration of time (seconds). Figure 1.3.b shows the glass cap and the polysilicon microheater ring.

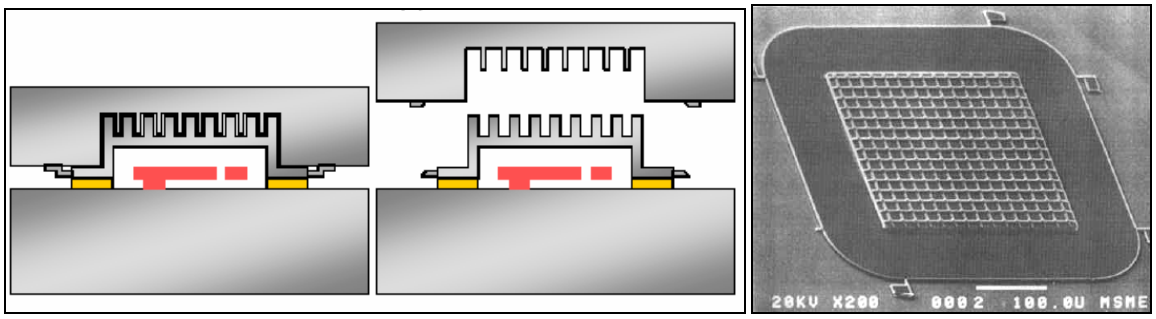


(a) (b)

Figure 1.3. Local bonding example: (a) View of the Al/Si bond ring around the resonator, b) View after breaking the cap [19].

Metallic bonding can be used to transfer a metal cap, called a microcap, from another wafer to the host MEMS wafer [6]. Figure 1.4.a shows a gold microcap transferred by Si-Au eutectic bonding [21]. The cap is created by etching the stiffening ribs and the main cavity, followed by depositing the sacrificial Phosphosilicate Glass (PSG), and refilling

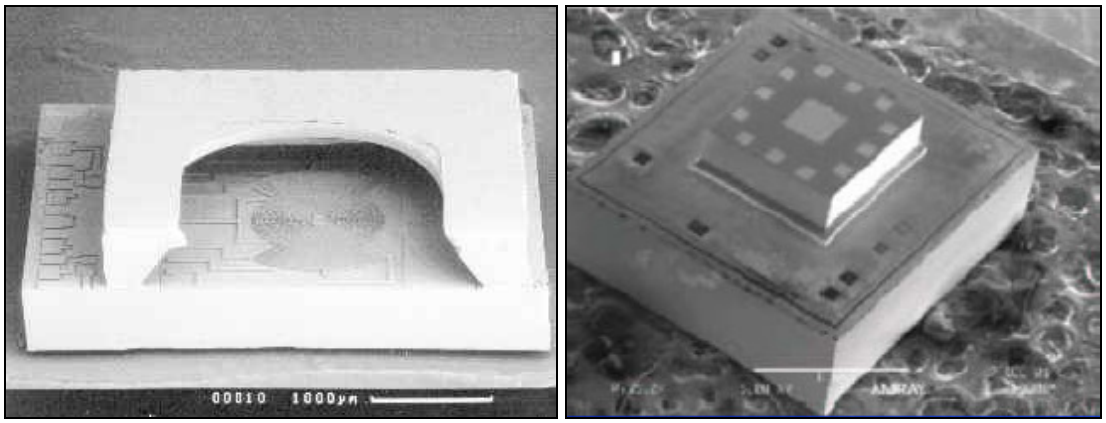
with gold. Then gold is bonded to the host MEMS wafer and the PSG is removed in HF, as shown in Figure 1.4.b. A Scanning Electron Microscope (SEM) view of the bonded micro-cap is also shown in Figure 1.4.c. Another method involves transfer of a nickel microcap using sacrificial solder and transient liquid phase bonding.



(a) (b) (c)

Figure 1.4. Hexsil microcap transfer: (a) Cap formation and bonding, b) Cap release, c) SEM of the bonded MEMS via microcap bonding [21].

Figure 1.5 shows two examples of wafer-level packaged MEMS sensors. Figure 1.5.a is a packaged gyroscope from Bosch using glass-frit-to-silicon bonding [22]. The gyroscope cap is opened to allow insight to the core element. Figure 1.5.b is a wafer-level packaged accelerometer from Analog Devices Inc. (ADI), where a silicon cap is bonded on top of the MEMS sensor and the interface circuit [23].



(a) (b)

Figure 1.5. (a) Bosch packaged gyroscope [22], b) ADI packaged accelerometer [23].

Wafer bonding results in good life expectancy, but has a number of disadvantages. First, the anchor region where the cap seals to the MEMS die must be huge to ensure a safe and hermetic seal, which translates into a significant increase in die size and die cost, and more important for the RF MEMS, an increase in electromagnetic loss. This is therefore directly related to the cost per device. Second, the bonded die is thicker than the standard IC die and the thickness of the total product is too thick for standard SOP packages. Moreover, it is difficult and costly to run non-standard sized chips through a lead-frame mounting or plastic molding line because process steps have to be changed and specifically adapted to the application. There is also a non-negligible risk of breaking the seal by the stress during mounting and molding, which is acting onto a large and massive cap. Third, wafer-to-wafer bonding requires alignment of the cap to the host MEMS wafer, which can complicate the packaging especially for small packages Also bonding requires clean wafer surfaces, so packaging of MEMS with rough surfaces with any type of cap bonding may be difficult and result in a non-hermetic seal and yield loss. It would be a significant advantage if a cheaper technology could be found that would lead to the same or a better performance/lifetime.

1.1.2. Sacrificial-Layer-Based Sealing Techniques

A possible alternative for cap bonding is the formation and sealing of surface micro-machined membranes over the MEMS. The advantage of this integrated packaging technique would be the reduced thickness and area consumption and the promise of being a lower-cost batch process. In these methods, a layer of sacrificial material (inorganic or organic film) is deposited, followed by the deposition of the overcoat layer by CVD or epitaxy. Then, small perforations are created in the overcoat, either by lithography or by

making the overcoat porous. The sacrificial material is etched (dry or wet) and finally another layer of overcoat is deposited to bridge over the small openings and create a rigid shell [15]. The inorganic thin-film packages include polysilicon, silicon nitride, silicon carbide and diamond [24-27].

Figure 1.6 shows a thin-film vacuum sealed MEMS pressure sensors [24]. The SEM of a sealed resonator is shown in Figure 1.6.a and the process flow is demonstrated in Figure 1.6.b. The sacrificial layer is boron doped polysilicon and the thin-film capsule consists of heavily boron-doped epi-polysilicon.

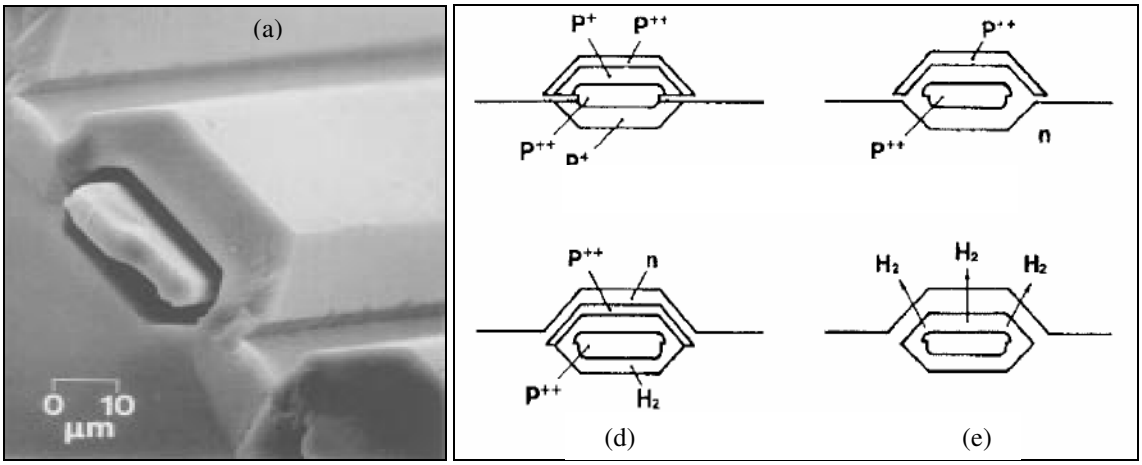
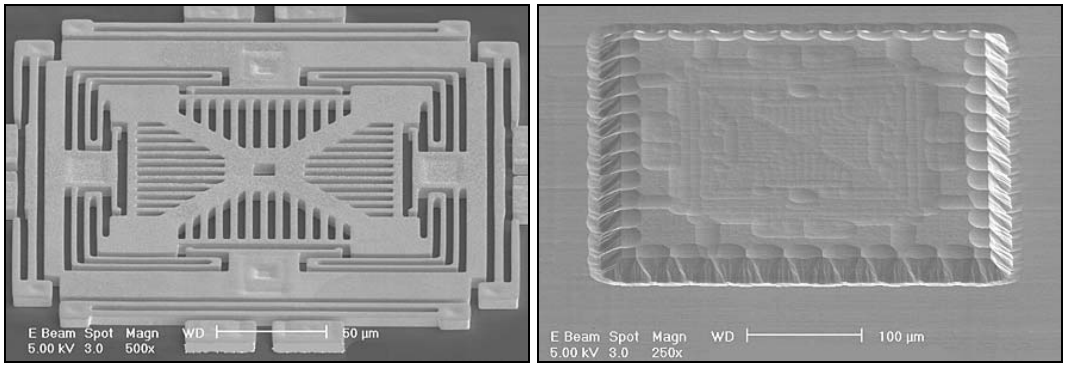


Figure 1.6. (a) Cross-section of the sealed resonator, b) Process flow for fabrication and packaging of the resonator: g) After selective epi (P+ and P++) and removing SiO2, (h) After selective etching, (i) Epi (n), (j) Annealing in N_2 [24].

After removal of the sacrificial layer, the final vacuum sealing is performed in two steps. The etch holes are sealed in the epi-polysilicon reactor, followed by outgassing of the remained hydrogen in the capsule by thermal permeation in a high-temperature LPCVD furnace and annealing in a nitrogen purged furnace at about 10 mT pressure.

A wafer-level thin-film packaging method has been proposed in [25], that seals the structure under a thin-film (30 μm) cap deposited during wafer manufacturing, as shown

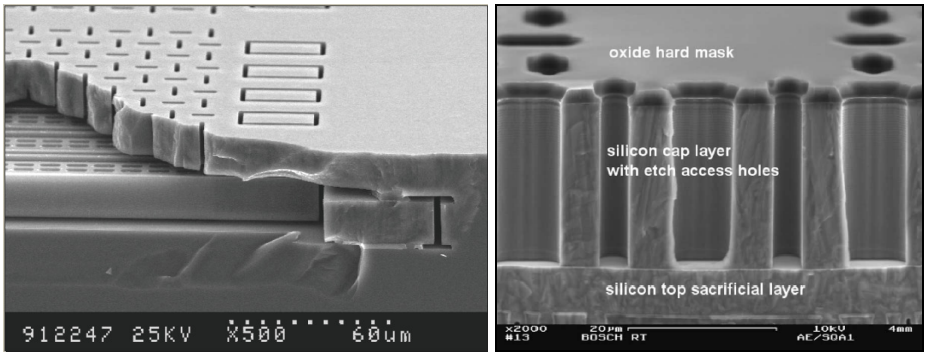
in Figure 1.7.a and 1.7.b, for an accelerometer before and after capping. The thin-film cap is deposited as one of the last steps of wafer manufacturing. It hermetically seals the MEMS structure and is sturdy enough to withstand the rigors (pressures up to 1500 psi and temperatures as high as 175°C) of the plastic injection-molding process.



(a) (b)

Figure 1.7. (a) A 3-axis MEMS accelerometer before capping, (b) The accelerometer after capping with a thin-film cap to hermetically seal the structure [25].

A similar technique has been used by epitaxial growth of polysilicon as the overcoat on top of the sacrificial PSG, as shown in Figure 1.8 [26]. Perforations are made in the cap and the sacrificial PSG is etched using vapor HF to avoid stiction of the overcoat to the accelerometer. These perforations are then bridged over by depositing Plasma Enhanced CVD (PECVD) glass, and finally the bonding pads are opened using pad holes.



(a) (b)

Figure 1.8. a) Packaged accelerometer [26], b) Perforations in the cap before sealing.

Sacrificial inorganic films that have been used for packaging include BSG, oxide, chromium, and copper. An example can be found in U.S. patent 5,589,082 by L. Lin *et al.* and is demonstrated in Figure 1.9 [27]. PSG defines the sacrificial material (about 7 µm), and 3 µm low-stress (silicon-rich) LPCVD silicon nitride with perforations is used as an overcoat, as shown in Figure 1.8.b. Besides LPCVD nitride, silicon carbide, and diamond have been used to define the shell for MEMS sealing [36].

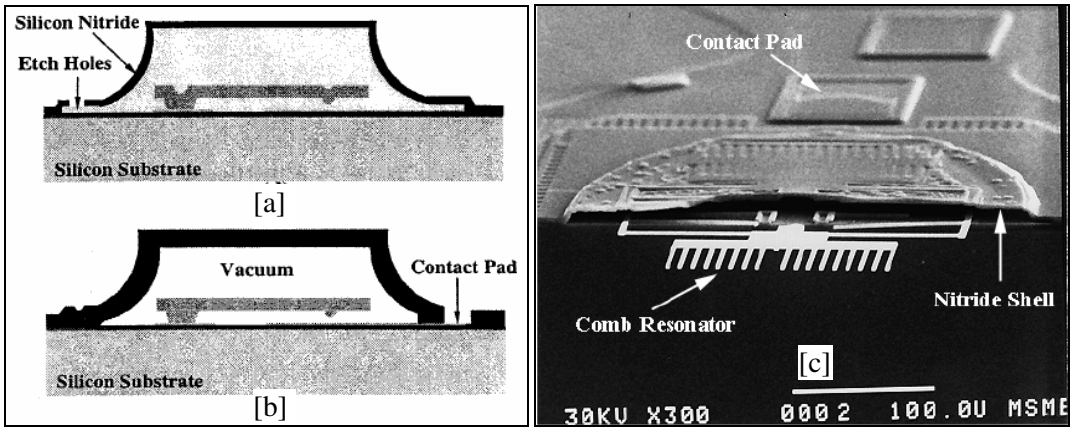
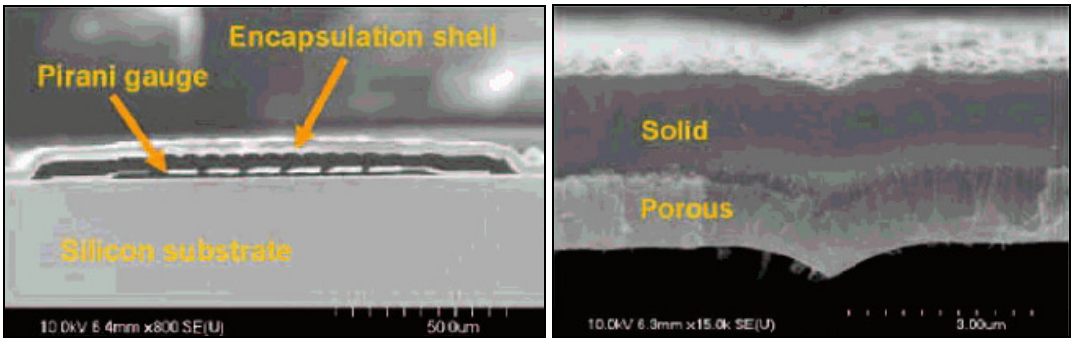


Figure 1.9. Vacuum packaging using sacrificial PSG, a,b) Process flow: a) After depositing 1m sacrificial PSG layer, 1 µm low stress nitride as the cap with etch holes, b) After removing PSG, filling the holes with 2 µm nitride and opening the pads, c) View of the packaged resonator [27].

Instead of using perforations in the overcoat, the overcoat can be made porous by electrochemical processing on LPCVD polysilicon, or by using a thin layer of polysilicon [28], as in Figure 1.10, or by using poly-SiGe [21], as shown in Figure 1.11.



(a) (b)

Figure 1.10. Vacuum packaging using porous polysilicon, a) View of the polysilicon cap, b) Closer view showing the solid and porous sections of the cap [28].

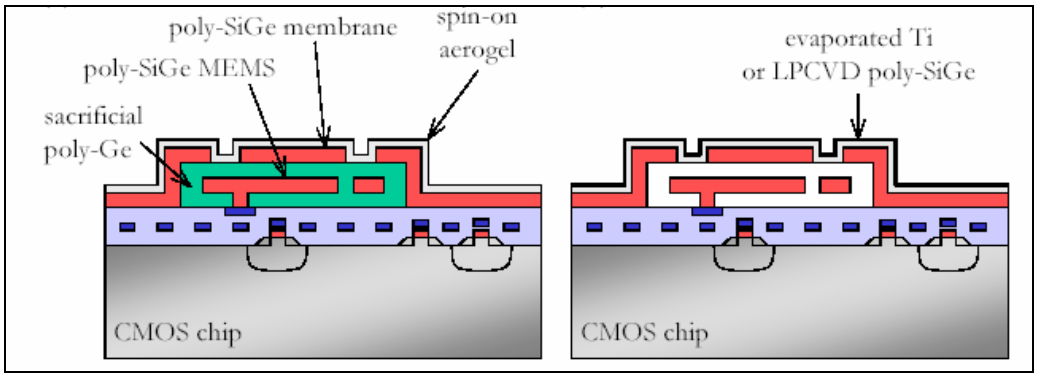


Figure 1.11. Process flow for the permeable poly Si-Ge packaging: a) Before sacrificial etching, b) After removal of sacrificial material and final sealing [21].

Other high and low temperature sealing methods include electroplating metals over sacrificial photoresists to be stripped in acetone [29], reactive gas sealing process [30], frozen water process [31], and polymer encapsulation [32]. In the reactive gas sealing, a polysilicon cap is formed on top of MEMS and then the cap is oxidized at 900°C to consume the gas inside the cavity and create partial vacuum. The frozen water process is based on evaporation of frozen water through a photoresist curable at room temperature. To pattern the frozen water, hydrophobic and hydrophilic regions should be defined to allow water to be selectively attached to the hydrophilic area under the ambient environment [31]. In the polymer encapsulation technique, instead of bonding the cap, the boundaries of MEMS device are protected by a glass microcap with a cavity and then a semi-hermetic thermoplastic, such as LCP is dispensed on top of the cap, as depicted in Figure 1.12. (similar to glob-top epoxy sealing used in microelectronics packaging). LCP has the lowest dielectric constant (2.49) and loss tangent (0.002) among all polymers and is attractive for RF MEMS packaging. Also LCP has near hermetic properties to achieve a low nitrogen permeability of 0.027 Barrer (for 2 mil thick LCP) and small moisture absorption [32]. Barrer is the permeability represented by a flow rate of 10^{-10} cubic

centimeters per second, times 1 centimeter of thickness, per square centimeter of area and centimeter of mercury difference in pressure. (1 Barrer = 10^{-10} $cm^2 \cdot s^{-1} \cdot cmHg^{-1}$).

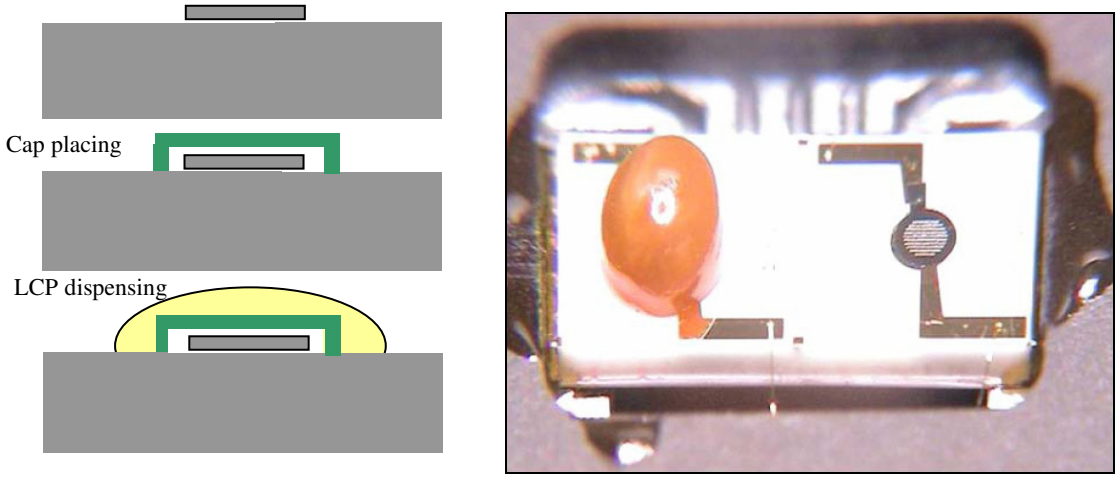


Figure 1.12. a) Process flow for LCP encapsulation, b) Humidity sensors with (left) and without (right) LCP encapsulation [32].

Another process used by Lockheed Martin is shown in Figure 1.13 [33]. The MEMS device is flipped and bonded into a Kapton wafer using epoxy as intermediate layer, followed by polymide coating at the backside. Finally, interconnects are made in the Kapton cap by patterning and etching. This method is not hermetic.

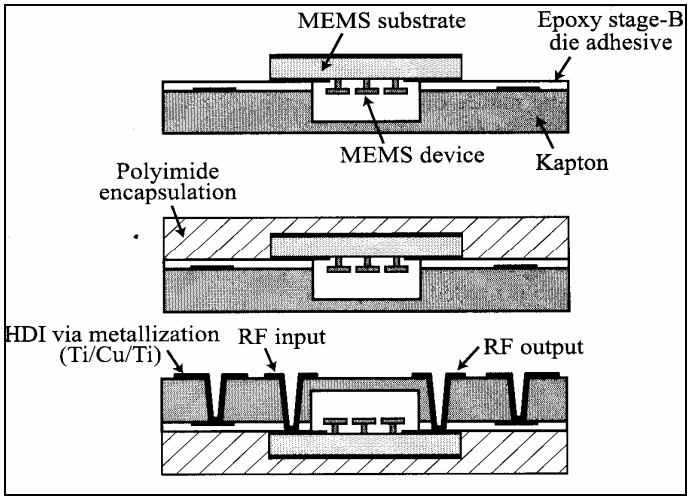


Figure 1.13. Polymide encapsulation method from Lockheed Martin [33].

1.1.3. Getters in MEMS Packaging

In all the mentioned packaging methods, ultimately surface desorption after sealing limits the cavity pressure. For bonding methods using intermediate layers, pressure will be gradually increased because of metal interdiffusion or polymer outgassing from the seal layer. Same thing holds for the sealing packaging approaches. To maintain the suitable vacuum level or to sorb gases inside the package, a micropump, called non Evaporable getter (NEG) can be installed [34]. The NEG coatings (sintered pills of metals and alloys, such as Ti, Zr, and Fe) have high porosity to sorb the gases. The NEG is activated in vacuum by heating to elevated temperatures (e.g. 350°C) to remove the protective oxide on the getter surface. Thin film getter deposition is also reported [35].

1.1.4. Interconnections in MEMS Packaging

MEMS packages must provide a convenient electrical, optical, fluidic, and chemical interface to the outer world. The electrical interconnect must be low-loss and have low resistive, capacitive, and inductive parasitics. Interconnects are one of the main mechanisms for packaging failure. In general, electrical interconnects can be divided into vertical and horizontal feedthroughs. Horizontal feedthrough is one of the easiest ways to access the MEMS pads, e.g. polysilicon feedthroughs in the glass bonded packages (Figure 1.14.a). Vertical feedthrough can be made inside the cap, or the host MEMS substrate using through-wafer vias. Figure 1.14.b shows feedthroughs in solder balls deposited over through-wafer vias to get access from the substrate backside [36]. The main limitation of this method is the minimum size of the holes that can be made. Figure 1.14.c shows vertical feedthrough made by through-wafer vias in the ceramic cap [37].

Also pad holes can be made in the cap to get direct access to the bonding pads. Pad holes are efficient for surface micromachined thin-film caps (Figure 1.14.d) [100].

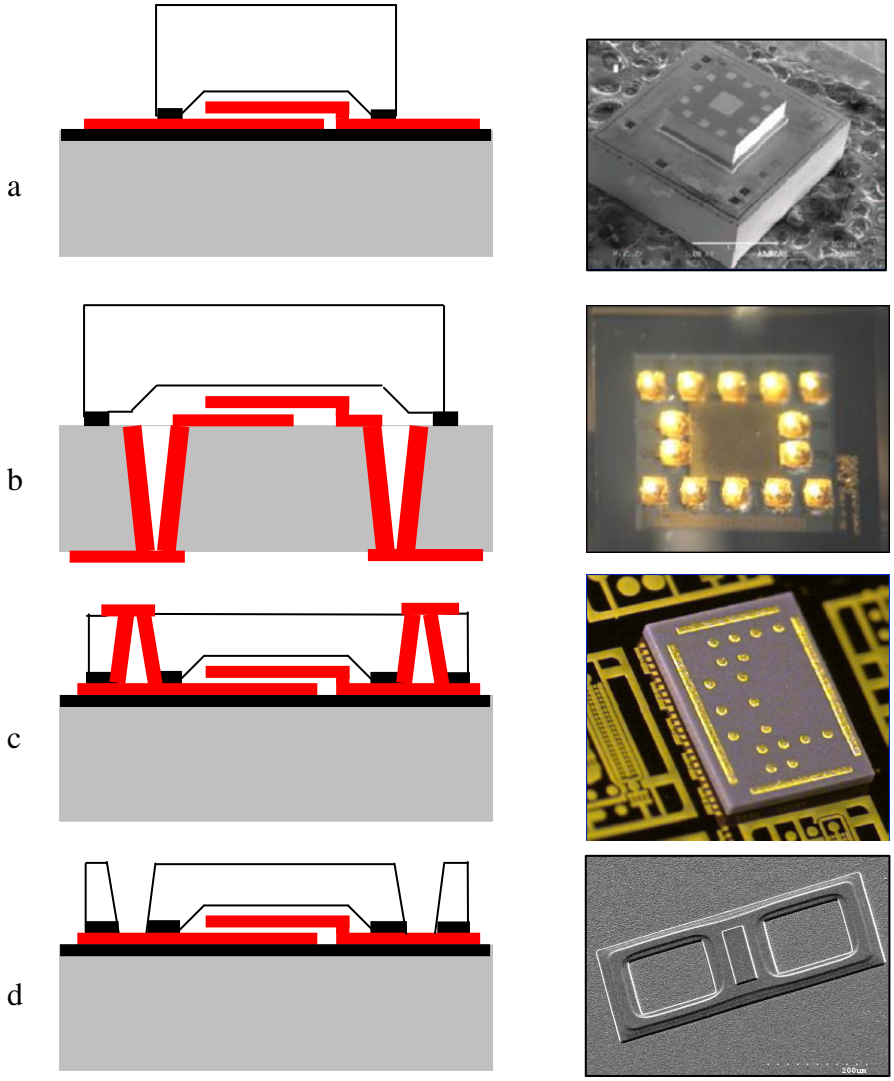


Figure 1.14. Classification of MEMS interconnections: a) Horizontal feedthrough, b) Vertical feedthrough in the substrate [36], c) Vertical feedthough in the cap [37], d) Vertical padholes in the cap.

1.2. Review of High-*Q* MEMS Tunable Capacitors

High-*Q* MEMS tunable capacitors have attracted a great deal of interest because of their lower loss and higher tuning range compared to solid-state varactor diodes [38-52]. Solid-state varactor diodes do not have any special packaging requirements, but they can not handle high power and can not have high tuning ranges together with high quality-factors at millimeter wave frequencies. Small size and high-*Q* MEMS variable capacitors can handle RF power swings and therefore result in very high linear tunable networks. The potential applications are in tunable filters, VCO, LNA, phase shifters, and antenna tuners. Figure 1.15 shows a superheterodyne transceiver with potential application areas for MEMS varactors.

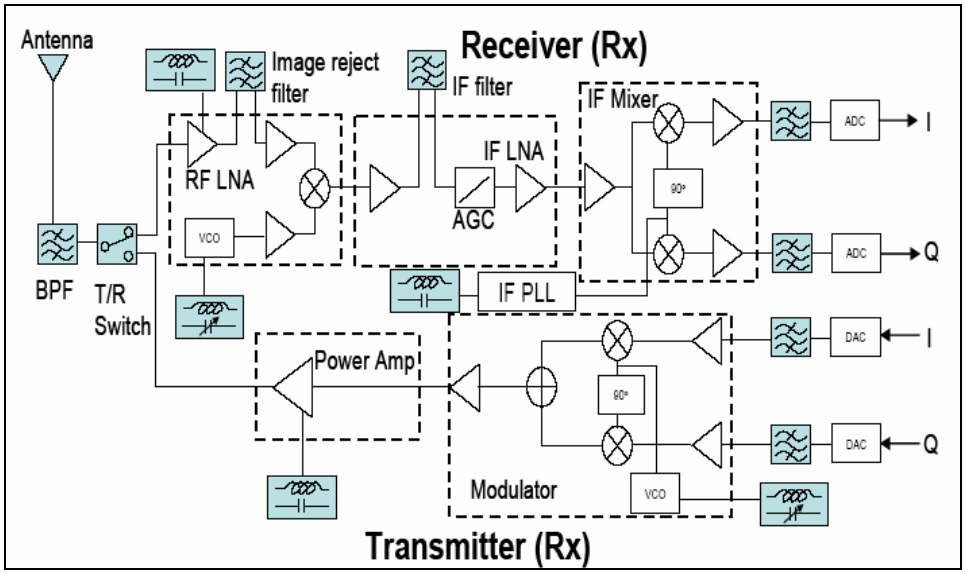
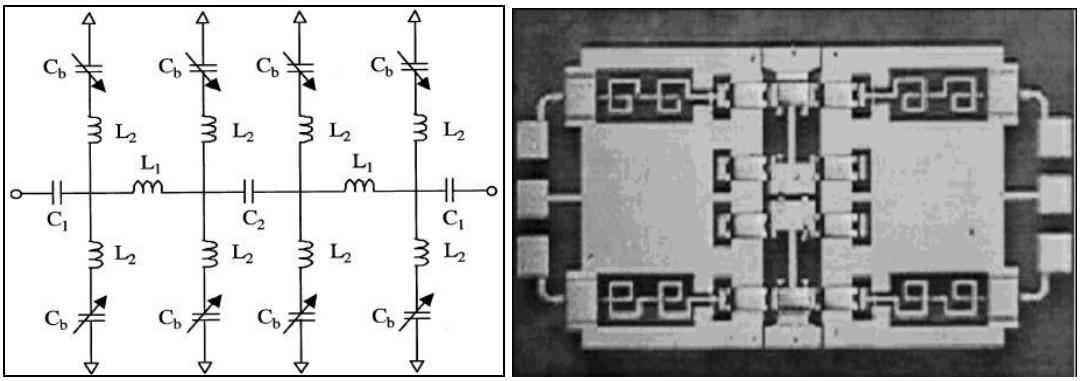


Figure 1.15. A superheterodyne transceiver with highlighted areas for the MEMS varactors.

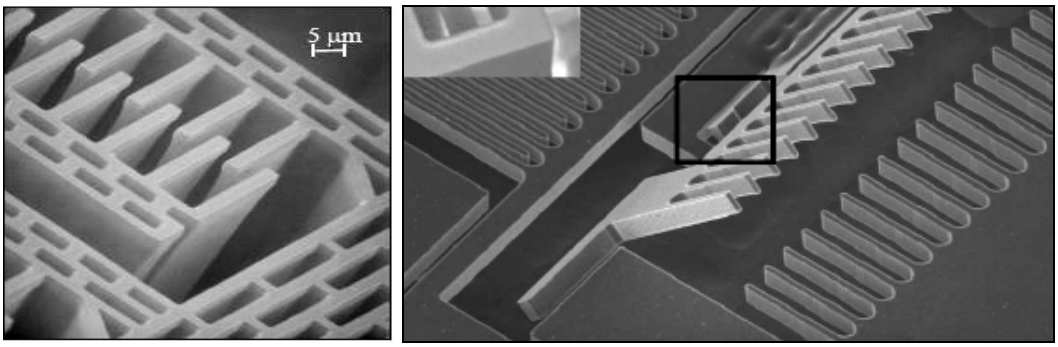
Shown in Figure 1.16 is an LC resonator-coupled tunable filter for V-band using varactors with a frequency tuning bandwidth of 10% [38]. The varactors and inductors are made by gold electroplating on a quartz substrate.



(a) (b)

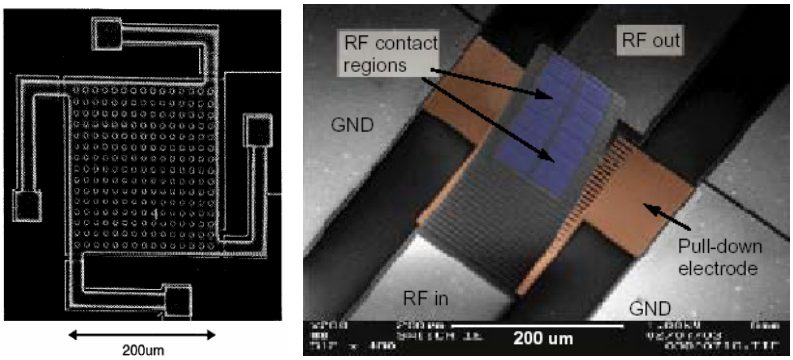
Figure 1.16. A MEMS analog tunable filter using MEMS varactors and inductors: a) Schematics of the bandpass filter, b) SEM of the fabricated circuit [51].

MEMS varactors can be classified as area-tuning, gap-tuning, or dielectric tunable capacitors. Examples of area/gap tuning are shown in Figures 1.17 [43, 52] and 1.18 [38, 49]. The gap tuning is the easiest method to implement tunable capacitors.



(a) (b)

Figure 1.17. Example of area variable interdigitated varactors in silicon (a) In-plane varactor [43], (b) Area variable angular varactor [52].



(a) (b)

Figure 1.18. Example of gap variable varactors: (a) Parallel plate [38], (b) Curled cantilever [49].

In gap-tunable capacitors, the major challenge is obtaining low tuning voltage [38]. One solution is to use folded plates, where the gap between the capacitor is smaller than the actuator [38]. Gap-tuning capacitors have been made using the microelevator by self-assembly (MESA) method [39]. The other method uses a digitally tuned capacitor [40] in which, after applying a voltage higher than the pull-in voltage on separate plates with different spacing, individual plates will touch the dielectric layer on the bottom layer. Piezoelectric actuation has been reported in [41]. Also, the zipper technique has been used in which a voltage is applied on a separated bottom electrode; the top solid electrode, which is put on top of the flexible polymer, will bend toward the substrate and results in decreasing the gap [42]. Area-tunable varactors have higher tuning ratio, but they may need higher tuning voltage. Examples of comb-driven capacitors have been presented with capacitive [43] or electrothermal actuations [44]. Achieving high Q is also possible by changing the dielectric permittivity [45-48]. A summary of high-tuning range MEMS varactors is given in Table 1.2 and Figure 1.19.

Table 1.2. High-Q MEMS tunable capacitors.

TCAP	Q, Frequency	Type	Year	Tuning range/Voltage
S. Kang *et al.* [38]	256, 1 GHz	Electrothermal actuator	1998	90%
C.T. Nguyen *et al.* [50]	218, 1 GHz	Movable dielectric	2000	90%
J. U. Bu, *et al.* [41]	210, 1 GHz	PZT actuator	2001	3:1
V. M. Bright, *et al* [40]	140, 750 MHz	Electrostatic	2001	4:1
J.F. DeNatale *et al.* [43]	100, 400 MHz	In-plane comb	2003	740%, 8 V
J. Muldavin *et al.* [49]	Not given	Curled cantilever	2004	3000%, 50 V
M. C. Wu *et al.* [52]	273, 1 GHz	Angular vertical comb	2003	3000%, 40 V
Monajemi *et al.* [96]	50, 1 GHz	In-plane parallel plate	2005	100%, 2 V

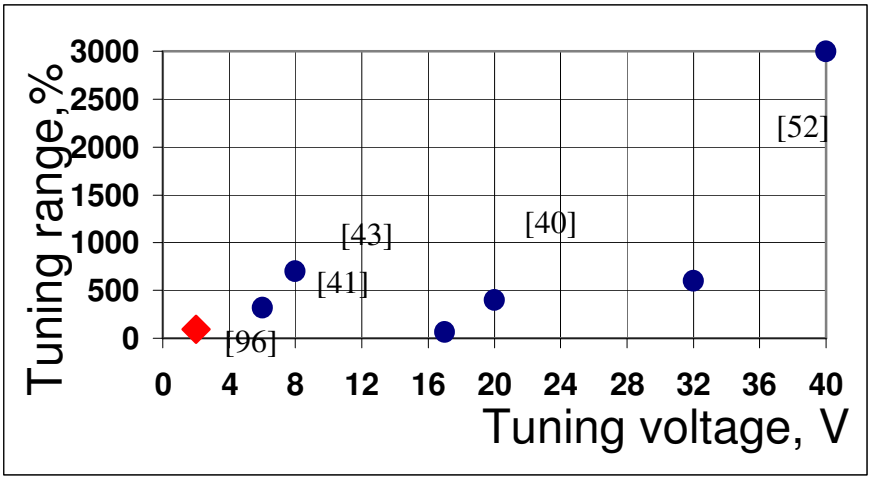


Figure 1.19. Graphical summary of MEMS varactors with high tunability.

1.3. Review of High-Resolution Silicon Inertial Sensors

Microaccelerometers have the second largest sales volume among MEMS after pressure sensors, with the automotive industry being the main user [53, 54]. Specific challenges for MEMS sensors include the release of 3D microstructures, added fragility resulting in the need for special handling and packaging, and testing of these devices [55]. Different designs are based on several physical mechanisms: capacitive, piezorezistive, electromagnetic, ferroelectric, optical, and tunneling [56-58]. Capacitive sensors have the advantage of design simplicity, because of standard materials, low-power consumption, good dc response, and good thermal stability [56]. The disadvantage is their susceptibility to electromagnetic interference [59-63].

Capacitive accelerometers with noise floor levels as low as 0.18 μg/√Hz have been reported [51, 54]. Silicon accelerometers can be divided into three categories: surface micromachined, Silicon-On-Insulator (SOI) [67], and bulk micromachined sensors.

1) Surface micromachined accelerometers: These sensors often take advantage of monolithic integration with peripheral electronics to improve performance. The first device of this type was introduced as ADXL50 by Analog Devices Inc. (ADI) in 1993. This device has a 2 μm thick structure and a gap of 2 μm, a sense capacitance of 100 fF with 500×625 μm^2 in size, a sensitivity of 0.2 fF/g, and a noise floor of 10 mg/√Hz for the airbag inflating system in automotive applications. In 1999, an improved version, ADXL105 was introduced to the market with a noise floor of 225 μg/√Hz. In 2002, the ADXL203, a packaged CMOS integrated accelerometer, was introduced [68]. However, because of its small mass (<1 μ-g), the sensitivity is very low. The University of California at Berkeley reported a 4.5 fF/g sensor having resolution of 32 μg/√Hz (2 μg/√Hz in vacuum) [69]. It has a 3.6 μ-g proof mass, 2.3 μm gap, and 900 fF sense capacitance. Carnegie Mellon University has developed a device [70] that has a 1.4 μ-g mass, a 1.5 μm gap, 0.3 fF/g sensitivity, and a 50 μg/√Hz noise floor. Surface micromachined devices can be monolithically integrated with CMOS, but they have limited sensitivity because of their small mass.

2) SOI accelerometers: These types of sensors define the mass by using the device layer of an SOI wafer [71, 72] or both the device layer and the handle layer of an SOI wafer [65]. The accelerometer reported in [65] has a noise floor of better than 200 ng/√Hz and a sensitivity of better than 15 pF/g in a 0.65 mm^2 area.

3) Bulk micromachined accelerometers: Wet etching, DRIE and wafer bonding have made bulk micromachined accelerometers attractive because of the capability of building high aspect ratio structures. Several Z-axis and torsional sensors utilizing these

technologies have been reported [61, 64, 72-76]. They provide up to 10 pF/g sensitivity and 0.35~50 μg/√Hz noise floor utilizing the full wafer thickness or a stack of wafers.

Silicon gyroscopes can be used as an IC-compatible companion with accelerometers for inertial navigation purposes [77, 78]. Gyroscopes have broad applications: automobile stability control, robotic guided vehicles, and stabilization of pointing systems for antennas. The performance of MEMS gyroscopes has improved by a factor of 10 every two years. A typical navigation grade gyroscope has a bias stability of around 0.01 to 0.001 °/hr. A bias stability of 0.1-1 °/hr is needed to augment external inertial reference systems such as the Global Positioning System (GPS). The gyroscopes with 10 °/hr bias stability can be used in spacecraft rotation measurements. Silicon gyroscopes can be divided into two main categories: surface and bulk micromachined gyroscopes:

1) Surface micromachined gyroscopes: The first silicon gyroscope was introduced by Draper Labs in 1991 [79]. ADI commercialized an integrated z-axis gyroscope with 0.05 °/s/√Hz in 2002 [80]. The University of California at Berkeley reported a z-axis 6 μm thick polysilicon sensor with resolution of 0.01 °/s/√Hz operating at 70 mT integrated with 0.8 μm CMOS [81]. Thin-film gyroscopes suffer from residual stress and large damping.

2) Bulk micromachined gyroscopes: The University of Michigan has several designs, including a Single Crystal Silicon (SCS) ring vibrating gyroscope operating in air [82], a nickel vibrating ring gyroscope [77], and a polysilicon vibratory ring gyroscope [78]. Tuning fork gyroscopes have shown good mechanical resolution because of their heavy

mass [83]. Carnegie Mellon University showed a DRIE CMOS-MEMS lateral axis gyroscope with a noise fl of 0.02 º/s/√Hz.

Georgia Institute of Technology has developed a z-axis tuning-fork gyroscope on 50-µm thick SOI substrate. For this sensor, the measured rate sensitivity is 24 mV/º/s, the angle random walk is 0.045º/√hr, and the bias instability is 0.96 º/hr [83].

In summary, a huge amount of effort has been focused on developing precision inertial sensors and the above examples only demonstrate a small portion of the advancements in the MEMS sensor technology.

CHAPTER II

DESIGN AND FABRICATION OF HARPSS ACCELEROMETER

With silicon as the major substrate material, many micro and nanostructures use trench-refilled polysilicon as their structural material because of its stress-free nature, high strength, and good thermal matching to the substrate.

2.1. Design and Analysis of HARPSS Silicon Accelerometer

The diagram of the in-plane (*X*-axis) HARPSS accelerometer is depicted in Figure 2.1. The device has a perforated silicon mass suspended by four tethers. The sense and feedback electrodes are made of trench-refilled polysilicon. The separation of each set of fixed/mobile electrodes is much larger than the gap spacing to enhance the sensitivity.

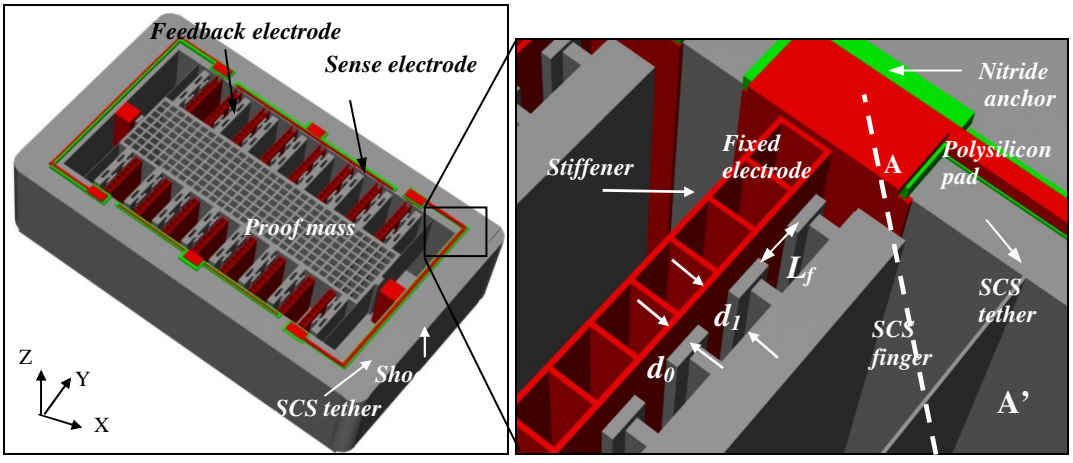


Figure 2.1. Diagram of the *X*-axis HARPSS accelerometer showing the electrodes, tethers and shock stops [84].

The SCS movable fingers have T-type corrugations to control the air damping. The large gap (d_1) is much larger than the sense gap (d_0) (see Figure 2.1). A set of local (out of plane, Z axis) and global (in-plane, X axis) shock absorbers has been placed to increase the shock resistance in those directions. Listed in Table 2.1 are the target specifications for the proposed Micro-g capacitive accelerometer.

Table 2.1. Target specifications for the micro-g accelerometer

Target Specifications	
Resolution in atmosphere	< 1μg/√Hz
Electronic Sensitivity	>10pF/g
Open Loop Bandwidth	1-100Hz
Non-linearity	<1%
Dynamic Range	>120dB
Shock Resistance	> 10,000g
Temperature Range	-40°C to 80°C

2.1.1. Geometry and Gap Optimization Method to Minimize Total Sensor Noise

The total noise equivalent acceleration (*TNEA)* of a capacitive accelerometer consists of mechanical and electrical components, as described in equation (2.1) [84]:

$$TNEA = \sqrt{MNEA^2 + ENEA^2} = \sqrt{\frac{a_{Mechanical}^2}{\Delta f} + \frac{a_{Electronics}^2}{\Delta f}} = \sqrt{\frac{4kTD}{M^2} + (\frac{\Delta C_{\min}}{S})^2} \qquad (2.1)$$

Here $MNEA(a_{Mechanical})$ is the equivalent mechanical noise (acceleration), $ENEA$ ($a_{Electronic}$) is the equivalent electrical noise (acceleration), k is the Boltzman constant, T is the temperature, M is the mass of the sensor, D is the damping coefficient, ΔC_{min} is the circuit minimum resolvable capacitance change, and S is the static sensitivity of the accelerometer.

Assuming that the interface circuit can resolve ΔC_{min}=3 aF/√Hz, a minimum sensitivity of 10 pF/g is required to ensure that the minimum acceleration creates enough capacitance change within the circuit resolution. As stated by (2.1), *MNEA* depends on *D*,

which is a strong function of gap size. Increasing the gap size will decrease the noise. However, sensitivity decreases by increasing the gap size, so there is a compromise between small *MNEA* and large sensitivity. From the fabrication point of view, having sub-micron gap sizes may result in stiction. Because of technical issues in designing a closed-loop controller, the system has been designed to operate in open loop. For small deflections, sensitivity, *S* is expressed as [53]:

$$S = \frac{\Delta C}{a} = \frac{2C_0}{d_0\omega_0^2} = \frac{2\varepsilon_0 nNL_F}{d_0\omega_0^2}(\frac{H}{d_0}) \quad (\text{F/(m/s}^2)) \tag{2.2}$$

C_0 is the rest capacitance, ω_0 is the resonance frequency, and L_F is the finger length. According to (2.1), a large sensitivity is needed to reduce the *ENEA*. The sensitivity must be greater than the ratio of sensor resolution (*TNEA*) to circuit resolution (ΔC_{min}).

For a fabrication process in which the gap is defined by Deep RIE, the gap aspect ratio (H/d_0) is constant, and *S* is inversely proportional to d_0. However, in the HARPSS process, *H* and d_0 are independent of each other; therefore, *S* will be a function of (d_0^2).

The resonant frequency, f_0, can be stated in terms of mechanical and electrical stiffness:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{K_{mechanical} - K_{electrical}}{M}} = \frac{1}{2\pi}\sqrt{\frac{4EH(\frac{W}{L})^3 - \frac{2C_{Bulk}V_{DC}^2}{d_0^2}}{M}} \tag{2.3}$$

W and *L* are the width and length of tethers, V_{DC} is the driving voltage, *E* is the effective Young's modulus of silicon and can be expressed as the Young's modulus and Poisson ratio, ν, as in equation (2.4) [85] . For [110] direction, $E_{Si,}$=169 GPa and ν=0.0625.

$$E = E_{Si}\{1+\frac{\upsilon^2}{1-\upsilon^2}\sum_{i=0} a_i(\frac{H}{L})^i\} \approx E_{Si}\{1+\frac{\upsilon^2}{1-\upsilon^2}(0.138+1.86(\frac{H}{L})-1.889(\frac{H}{L})^2)\} \tag{2.4}$$

We have proposed a method for deceasing the air damping without vacuum packaging [84]. Figure 2.2 shows the basic and corrugated electrode configurations.

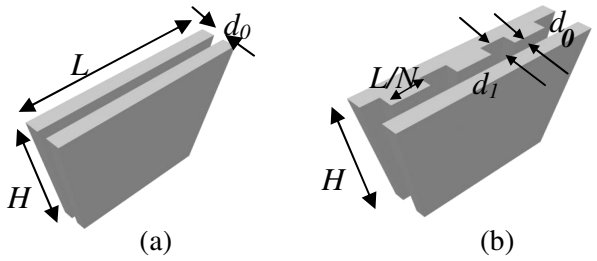


Figure 2.2. Electrode configurations: (a) Basic, and (b) Corrugated.

The cavity gap (d_1) is much larger than the sense gap (d_0). A similar method has been used to design corrugated vibration sensors [85-90]. For the basic scheme (assuming $L>H$), D can be stated as in equation (2.5) [85]:

$$D = \mu_{\text{Eff}}\, nL\left(\frac{H}{d_0}\right)^3 f\left(\frac{H}{L}\right) \qquad \text{(Ns/m)} \qquad (2.5)$$

Where μ_{Eff} is the effective viscosity of air molecules, d_0 is the sense gap, H and L are the height and length of electrodes, respectively, with $L>H$; n is the total number of electrodes and $f(x)$ is a nonlinear function, explained in [90]. For low-frequency excitations and for slip regime of operation, μ_{Eff} can be modeled by (2.6) where λ_{air} is the mean free path of air molecules [85]:

$$\mu_{Eff} = \frac{1.8\times10^{-5}}{1+9.638\left(\frac{\lambda_{air}}{d_0}\right)^{1.159}} \qquad \text{(Kg/ms)} \qquad (2.6)$$

Assuming there is no damping correlation in the individual fingers and neglecting turbulence, the damping for n set of N-corrugated fingers ($L_i<H$) is written as following:

$$D = \mu_{Eff}\, Hn \sum_{i=1}^{N} \left(\frac{L_i}{d_0}\right)^3 f\left(\frac{L_i}{H}\right) \qquad \text{(Ns/m)} \qquad (2.7)$$

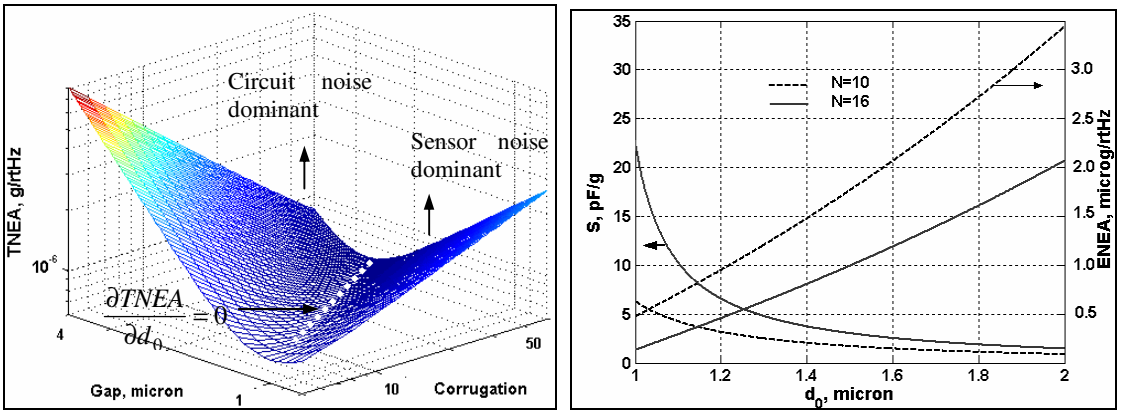
For $L<0.5H$, the nonlinear function, f can be approximated by the following [90]:

$$f(x) \cong 1 - 0.6x \tag{2.8}$$

In our design, $L_i<<H$ and therefore $f \cong 1$. By comparing (2.6) and (2.7), it can be seen that the corrugated-electrode damping is almost N^2 times smaller than the basic-electrode damping. It is supposed that damping of adjacent fingers is independent.

In our design, in order to minimize *TNEA,* both *MNEA* and *ENEA* have to be considered. Applying (2.7) in equation (2.1) proves that *MNEA* is a strong function of the gap spacing, d_0, and finger length, L_F, and *ENEA* is a function of *S*, which is dependent on gap size in our process. In the HARPSS process, gap size is definable with high precision, so the most efficient way to minimize *TNEA* is to find the optimum gap, $d_0(opt)$. By knowing *M* and realizable L_F, the optimum electrode length, or equivalently the number of corrugations, can be obtained.

The parameter of interest, *TNEA*, is plotted in Figure 2.3.a as a function of gap size and number of fingers for *M*=1 m-g, *n*=20. *S* and *ENEA* are plotted in Figure 2.3.b for a gap range of 1-2 μm assuming a mass of 1 mgr and a total stiffness of 10 N/m for *N*=10 and 16.



(a) (b)

Figure 2.3. (a) Plot of TNEA in [gap, N] domain for 20 electrodes/side, (b) Plot of *S* vs. gap size.

The solution to S>3 pF/g, $ENEA$<1 μg/√Hz is d<1.4 μm. Using (2.1)-(2.8) and taking H, K, ΔC, (nN), and L_F as known variables, the optimal gap, $d_0(opt)$, is stated in (2.9).

$$d_0(opt) = \left(\frac{24 kT \mu_{Eff} \varepsilon_0^2 (nNH)^3 L_F^5}{(K\Delta C)^2}\right)^{\frac{1}{7}} \tag{2.9}$$

This optimum value corresponds to $MNEA$=$ENEA$ and is expressed as in (2.10):

$$TNEA = \sqrt{2} MNEA = \frac{2\sqrt{4kT\mu_{\text{Eff}} Hn \sum_{i=1}^{N} \left(\frac{L_F}{d_0(opt)}\right)^3}}{M} \tag{2.10}$$

Applying $d_0(opt)$=1.3 μm in equation (2.10) using M =1 mg, H=60 μm, L_F=25 μm, K=10 N/m, μ_{Eff} =1.8×10^{-5} Nm/s, results $TNEA$=1 μg/√Hz.

2.1.2. Thermo-Mechanical Modeling of the Brownian Noise

The effect of corrugation on reducing the air damping can be verified by thermal simulation in ANSYS. The Reynolds' number for the small gap was calculated to be less than 0.04 for (d_0<2 μm), so the airflow in the small gap is laminar. In the large gap, since the velocity of the squeezed air molecules escaping out of the small gap is too small (10-100 μm/sec because of the small range of frequency; 0-10 Hz), and since the corrugated finger spacing is large (35 μm), the air molecules escaping from two opposite small gaps do not undergo collisions to create turbulence. Therefore, no turbulent/air compressibility effects will occur to correlate the damping forces. The pressure distribution, P, can be analyzed by Navier-Stokes equations (2.11), assuming small squeeze numbers, low-pressure variation and small deflection:

$$\frac{\partial^2 P}{\partial x^2} + \frac{\partial^2 P}{\partial y^2} = \frac{12\mu_{Eff}}{d_0^3} \frac{\partial z}{\partial t} \tag{2.11}$$

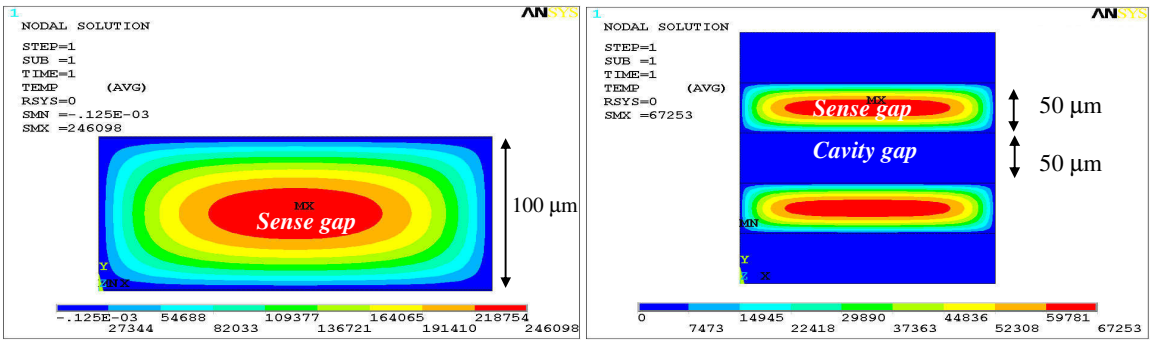
D can be calculated by integrating the pressure on the surface.

Reynolds' equation for squeeze film damping is analogous to Poisson's equation that defines heat conduction for temperature in two-dimensions, as stated in (2.12) (k is the thermal conductivity):

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} = \frac{1}{k}\frac{\partial q}{\partial t} \tag{2.12}$$

If we assume a constant velocity for the air molecules, equations (2.11) and (2.12) are the same if we change the temperature with pressure. In the steady state, by choosing a fixed velocity of 1 m/sec, that is analogous to dq/dt =1 W/m^3, D can be calculated. As shown in Figure 2.4, the maximum temperature for two corrugations is four times smaller than the non-corrugated design. To confirm the analytical calculations, we use:

$$k = d_0^3 / 12\mu_{Eff} \,. \tag{2.13}$$



(a) (b)

Figure 2.4. FEM analysis of air pressure distribution for a 1 µm sense gap and 10 µm cavity gap (perpendicular to the page) in: (a) Basic configuration; (b) Corrugated configuration [84].

Effect of fringing field on reducing the poly-Si/air/silicon capacitance is studied by electrostatic analysis in FEMLAB (Figure 2.5). This method gives a capacitance change of 19.67 aF for 0.1 µm movement (1 V DC), while calculation yields a change of 21.08 aF. A 20 µm long finger with a 1 µm sense gap, surrounded by 20 µm cavity gap results in about 7% reduction in sensitivity compared to the calculation neglecting fringing field.

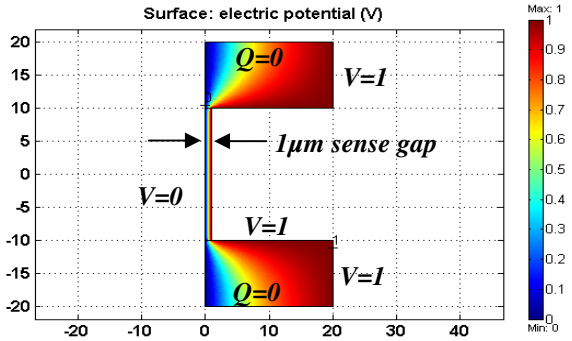


Figure 2.5. Potential distribution used to calculate the capacitance inside the 1 μm sense gap and 10 μm cavity for 1 V voltage difference between SCS and polysilicon [84].

Another important issue in the design is the cross-axis sensitivity, defined as the ratio of sensitivity in the transverse direction (S_Z) to lateral sensitivity (S_X), which is proportional to $(f_X/f_Z)^2$, as derived in eqaution (2.14). Separating the second-order resonance mode from the fundamental mode will decrease the off-axis sensitivity, which is possible by increasing the height-to-width ratio of the tether.

$$\frac{S_Z}{S_X} = \frac{(1/\omega_Z)^2}{(1/\omega_X)^2} = (\frac{f_X}{f_Z})^2 \tag{2.14}$$

The FEM modal analysis with 256 access holes occupying 35% of the total mass area shows a first resonance mode (f_X) at 427 Hz, as shown in Figure 2.6. The second resonance mode (f_Z) occurs at 3.4 kHz, which yields an off-axis sensitivity of about 1.5%. The perforated mass has less overall stiffness, compared to a solid mass.

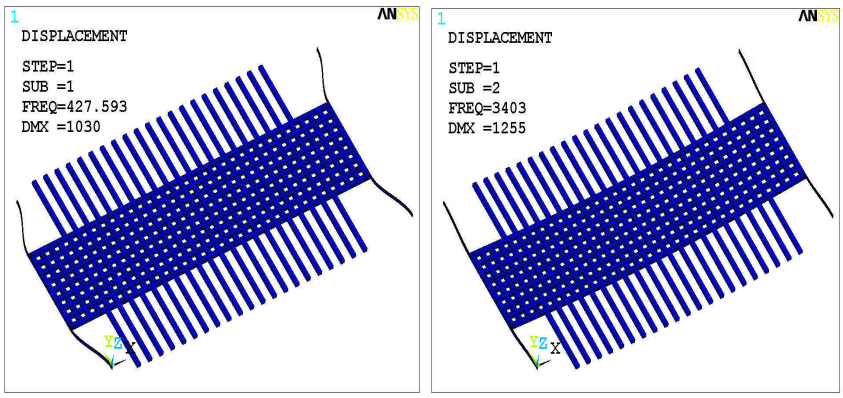


Figure 2.6. The 1st and 2nd modes (427 Hz and 3.4 kHz) of the optimized 60 μm thick sensor [84].

2.1.3. Distributed Finger Noise for the HARPSS Accelerometer

Figure 2.7 shows the distributed mass-spring system corresponding to the corrugated fingers. The *i'th* section can be modeled by a mass, M_i and stifness, K_i and the displacement of the section from the equlibrium is denoted by x_i.

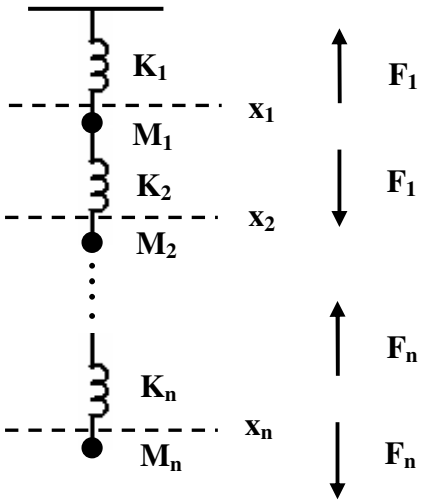


Figure 2.7. Representation of the distributed fingers in a HARPSS accelerometer

Neglecting the mass of the spring and assuming the spring to be linearly elastic, the dynamics of the system is governed by the following simple equations. (i=1, 2, …, n-1)

$$m_i \frac{\partial^2 x_i}{\partial t^2} = -K_i(x_i - x_{i-1}) - K_{i+1}(x_i - x_{i+1}) \tag{2.15}$$

$$m_n \frac{\partial^2 x_n}{\partial t^2} = -K_n(x_n - x_{n-1}) \tag{2.16}$$

Assuming m_j=m, equations (2.15) and (2.16) can be arranged equation (2.17):

$$\ddot{X} = A.X \tag{2.17}$$

where A and X matrices are defined in (2.18):

$$X = \begin{bmatrix} x_0 \\ x_1 \\ \bullet \\ \bullet \\ x_i \end{bmatrix} \qquad A = \begin{bmatrix} \frac{K_1}{m} & -\frac{K_1+K_2}{m} & \frac{K_2}{m} & 0 & \bullet & \bullet & \bullet & 0 \\ 0 & \frac{K_2}{m} & -\frac{K_2+K_3}{m} & \frac{K_3}{m} & 0 & \bullet & \bullet & 0 \\ \bullet & & & & & & & \\ \bullet & & & & & & & \\ \bullet & & & & & & & \\ 0 & 0 & \bullet & \bullet & \bullet & 0 & \frac{K_{n-1}}{m} & -\frac{K_n}{m} \end{bmatrix} \tag{2.18}$$

Assuming no damping and no external acceleration are present, the deflection of each individual finger, x_i, due to deflection of proof mass, x, can be derived as following:

$$0 = -Kx - K_1(x - x_1) \Longrightarrow x_1 = (1 + \frac{K}{K_1})x$$

$$0 = -K_1(x_1 - x) - K_2(x_1 - x_2) \Longrightarrow x_2 = (1 + \frac{K}{K_1} + \frac{K}{K_2})x$$

$$x_i = (1 + \sum_{1}^{i} \frac{K}{K_j})x \tag{2.19}$$

Therefore, the total damping can be calculated as in equation (2.20).

$$D_{Total}\frac{dx}{dt} = \sum_{1}^{n} D_i \frac{dx_i}{dt} = \sum_{1}^{n} D\frac{d}{dt}(1 + \sum_{1}^{i} \frac{K}{K_j}\frac{dx}{dt})x = D\frac{dx}{dt}(n + \sum_{i=1}^{n}\sum_{j=1}^{i} \frac{K}{K_j}) \tag{2.20}$$

Consequently, the total damping can be simplified as in equation (2.21).

$$D_{Total} = D(n + \sum_{i=1}^{n}\sum_{j=1}^{i} \frac{K}{K_j}) \tag{2.21}$$

Where D is assumed to be identical for all the fingers, as stated in (2.7) and (2.22).

$$D_{Total} = \mu_{\text{Eff}} H \sum_{i=0} H(\frac{L_i}{d_0})^3 f(\frac{L_i}{d_0}) = \frac{\omega_0 M}{Q} \tag{2.22}$$

In the trivial case where the fingers are made to be very stiff ($K >> K_j$), we get: $D_{Total} = nD$. Perforations should not have a detrimental effect on reducing the electrode stiffness, in other words, $K << K_j$ to avoid distributed finger noise from increasing the total damping. ANSYS simulation of Figure 2.8 shows deflection of an electrode due to 1 g gravity. Here $K_{electrode}$=12,000 N/m which is much larger than K_{spring}=10 N/m.

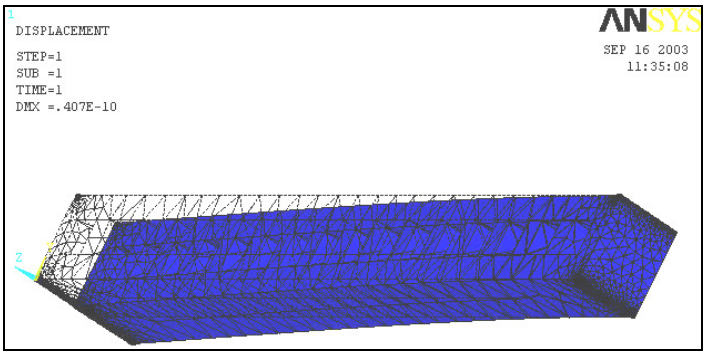


Figure 2.8. Static simulation of SCS electrode stiffness ($M_{electrode}$= 50 µg, $K_{electrode}$=12,000 N/m).

2.2. HARPSS in Silicon Fabrication Process for Inertial Sensors

The four-mask fabrication process flow, in particular the cross section of the electrode, mass, and tether area of an accelerometer/gyroscope or tunable capacitor, is shown in Figure 2.9. First, LPCVD silicon nitride is deposited on a low resistivity (<0.05 Ω-cm) silicon wafer for electrical isolation [91]. Then, the structural trenches are defined by DRIE, with a medium aspect ratio of 20:1 to define the thickness of the device, as used before to create isolation trenches on a regular silicon substrate [92]. Thermal oxide will be grown as the sacrificial material to define the high aspect ratio vertical air-gap, followed by trench-refill using polysilicon. Since the ratio of the oxide thickness to the SCS beam width is kept to less than 20%, the effect of stress resulting from oxidation on beams is negligible [93]. The fixed electrodes are formed by refilling the trenches with boron-doped polysilicon, followed by annealing to activate the dopants.

Oxidation of SCS has four major advantages over depositing LPCVD oxide: 1) Oxide growth enhances the surface roughness and *Q* of the SCS structures; 2) The uniformity of grown oxide film is 1:1 (top of trench:bottom of trench), while this figure is about 1:0.7 for an LPCVD oxide inside a 100μm trench; 3) Since there is no oxide grown on the nitride, poly will be directly anchored on nitride, eliminating the need to blanket-etch the first poly, open the oxide in the anchor area, and deposit a second layer of poly-Si, as in the original process. Polysilicon is consequently etched inside the isolation trenches that define the borders of SCS fingers, with sacrificial oxide as the mask. This requires a sequence of high-frequency (13.56 MHz) and low-frequency (380 kHz) plasma sources with gradual power ramping [94]. This step was performed in an STS DRIE tool.

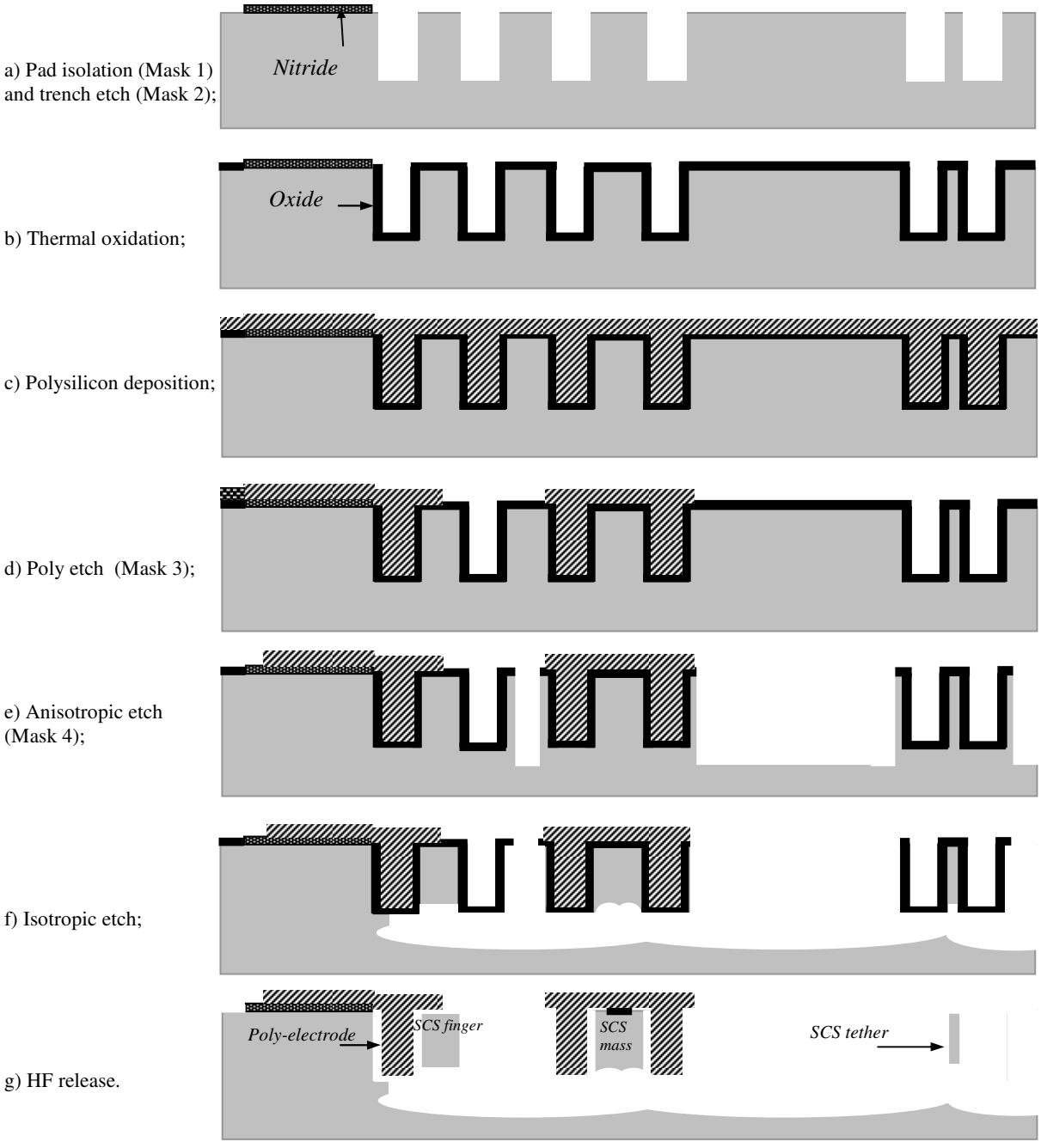


Figure 2.9. Process flow for the HARPSS sensors on regular silicon substrate [84, 95].

The low-frequency source is required to allow the long lifetime electrons to recombine with ions to neutralize the positive charge build up on the oxide sidewalls. The polysilicon in the proof mass area will be kept to increase the total mass by a factor of two. The moving structure is released by a combination of anisotropic and isotropic dry etch to undercut the device at the bottom. Finally, sacrificial oxide is removed in an HF/H_2O solution, followed by drying in a super critical dryer to prevent lateral stiction.

The main reasons for using SCS instead of poly-Si as the structural material are:

(1) SCS movable structures are void/stress-free, which is required for high-*Q* devices.

These result in high reliability, long lifetime, good thermal stability, and high shock resistance compared to methods using LPCVD polysilicon as the moving part [61, 64].

(2) Creating wide (>20 μm) beams is only possible using silicon from the substrate.

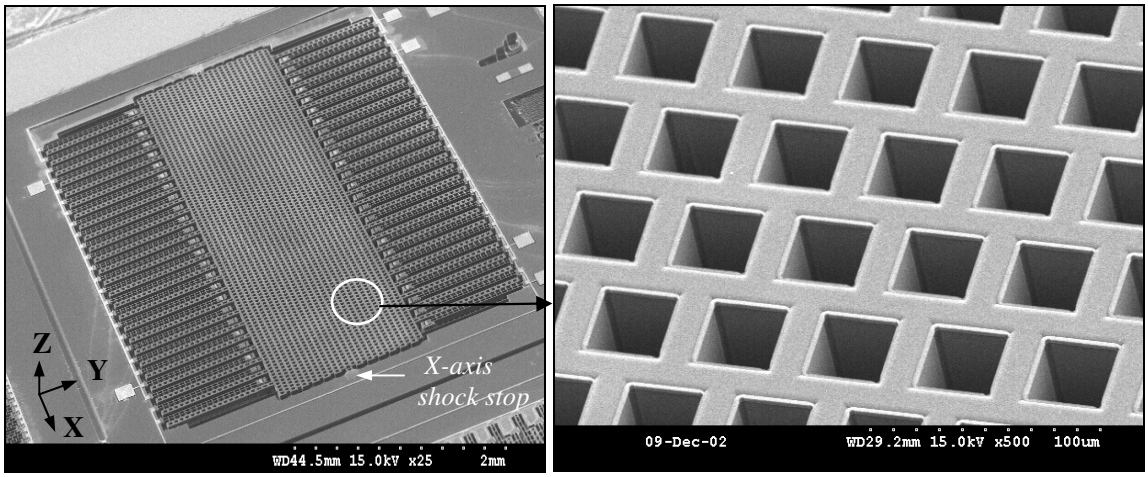
(3) The SCS suspended mass has higher shock resistance and fracture strength because it is directly connected to the substrate, as compared to polysilicon suspension of mass.

The process is a single-sided and single-wafer process, which eliminates the need for wafer bonding, double-sided processing on regular silicon wafers [64], or expensive SOI wafers [71]. The device thickness and the gap spacing can be varied over a wide range. This feature enables the implementation of higher aspect-ratio capacitors (>200:1) compared to DRIE technique [95].

2.3. Fabrication of the HARPSS Accelerometer

Prototypes of 30-100 μm thick accelerometers have been successfully fabricated and tested. The SEM view of a 60 μm thick device with 1.3 μm optimal gap are shown in

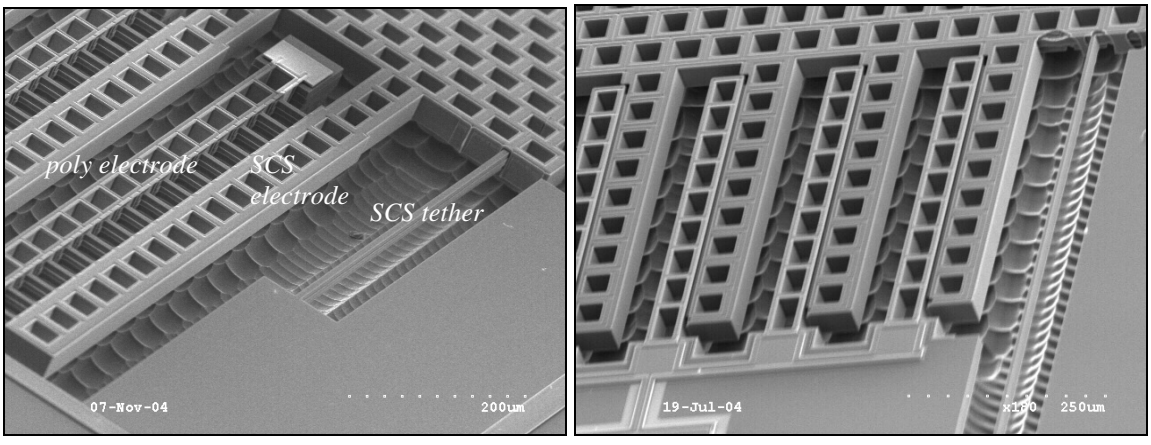
Figure 2.10.a. The sensor occupies an area of about 4 mm^2. The release hole size is 40 µm×40 µm, as shown in Figure 2.10.b.



(a) (b)

Figure 2.10. SEM View of the 60 µm thick HARPSS accelerometer [84].

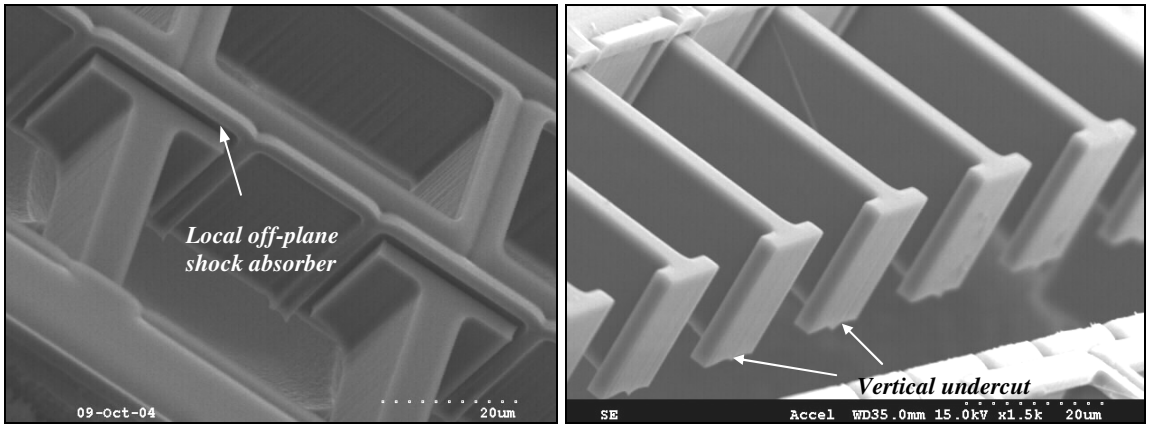
Figure 2.11 shows close-up views of tethers, electrodes, and anchors of two different designs. Figure 2.11.a is the corrugated clamped-clamped electrode design (n=16) and Figure 2.11.b is the non-corrugated clamped-free design (n=1). Removing the sacrificial oxide in HF is slower for the second design, since oxide is exposed to HF only from top and bottom.



(a) (b)

Figure 2.11. (a) View of (a) Corrugated electrodes, (b) Non-corrugated electrodes [84].

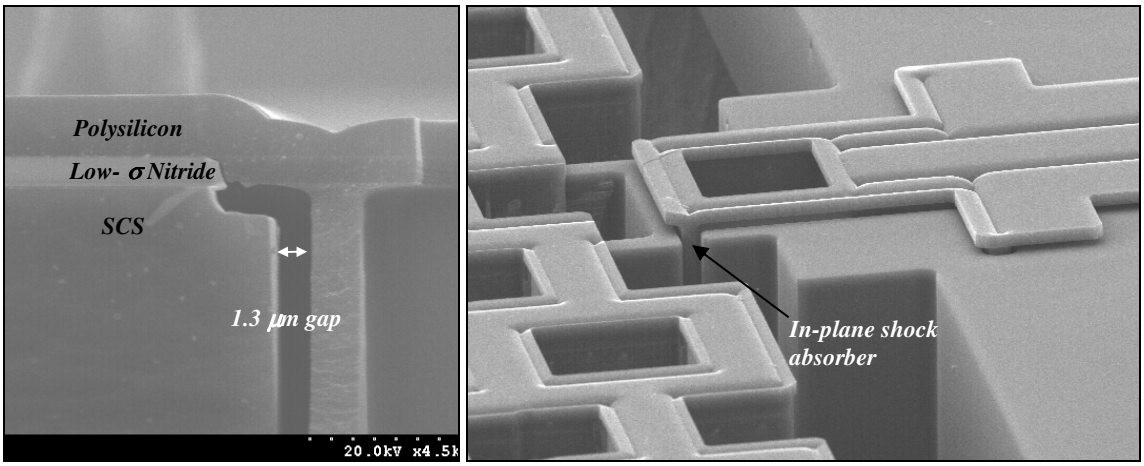
The SEM view of the electrode/finger area is shown in Figure 2.12.a. Creation of multi-axis shock absorbers is another unique aspect of the SCS HARPSS process. The polysilicon electrode covers the SCS fingers from the top and forms a local out of plane shock absorber, distributed in the entire sensor electrodes. The poly electrodes have been broken to verify the shape and surface roughness of the oxidized SCS fingers, as shown in Figure 2.12.b. The 25 μm wide SCS fingers are separated by 30 μm corrugations.



(a) (b)

Figure 2.12. (a) SCS fingers and off-plane shock absorbers, (b) View of the corrugated SCS fingers after breaking the poly-Si ladder electrodes [95].

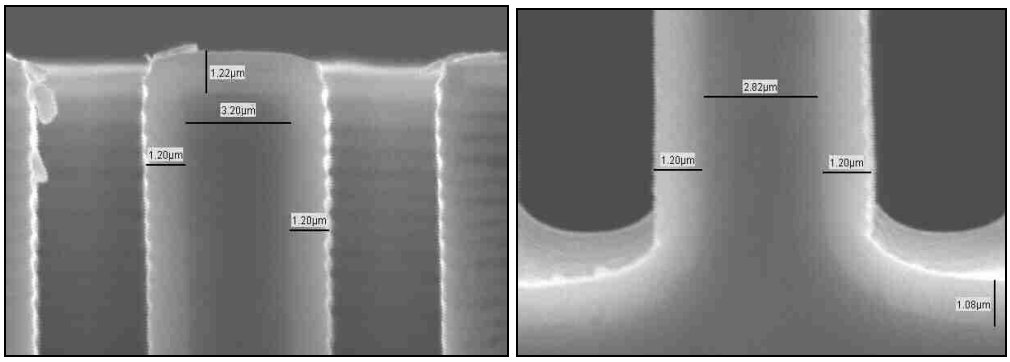
As shown in Figure 2.13.a, the fixed polysilicon electrodes are anchored on 1.1 μm low stress LPCVD silicon nitride (Appendix C). The sacrificial oxide thickness is 1.3 μm, as required by the design equations (2.9) and (2.10). Direct anchoring of polysilicon over nitride increases the surface area and creates more resistance against shear forces, at the price of larger pad capacitance. The SEM view of the global in-plane polysilicon shock absorber is illustrated in Figure 2.13.b. Both types of x-axis and z-axis shock stops tolerate 500 g of shock excitation. No shock absorber has been placed in the y-direction because of the large stiffness in that direction ($K_Y >> K_X, K_Z$).



(a) (b)

Figure 2.13. (a) SCS fingers and off-plane shock absorbers. (b) Cross section of the anchor area. (c) In-plane (*X*-axis) shock absorber [84].

Figure 2.14.a and b show the profile of the thermal oxide, grown over a 60 μm deep trench to verify the 1:1 uniformity. For LPCVD oxide, the top oxide is about 1.4 times thicker than the oxide deposited at the bottom.



(a) (b)

Figure 2.14. Profile of the 1.2 μm thick oxide grown on a 100 μm deep trench: a) Top of trench; b) Bottom of trench [95].

As mentioned in section 2.2, a thick sacrificial oxide grown at high temperatures on a long and narrow SCS beam can cause stress and beam buckling [93]. In order to verify this, 2 μm thick oxide was grown at 1000°C on an 8 μm wide, 800 μm long beam. As shown in Figure 2.15, a significant beam buckling can be observed after releasing the device.

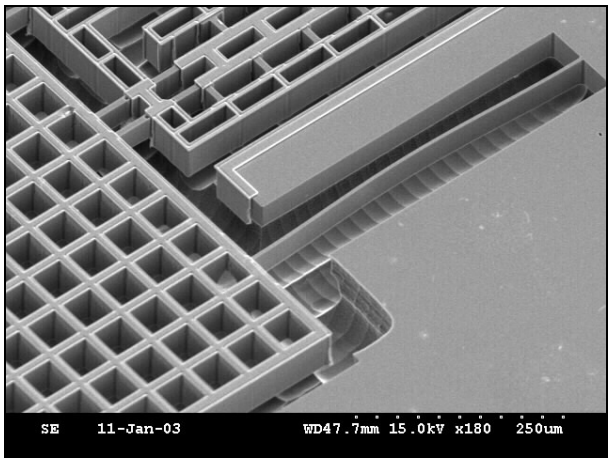
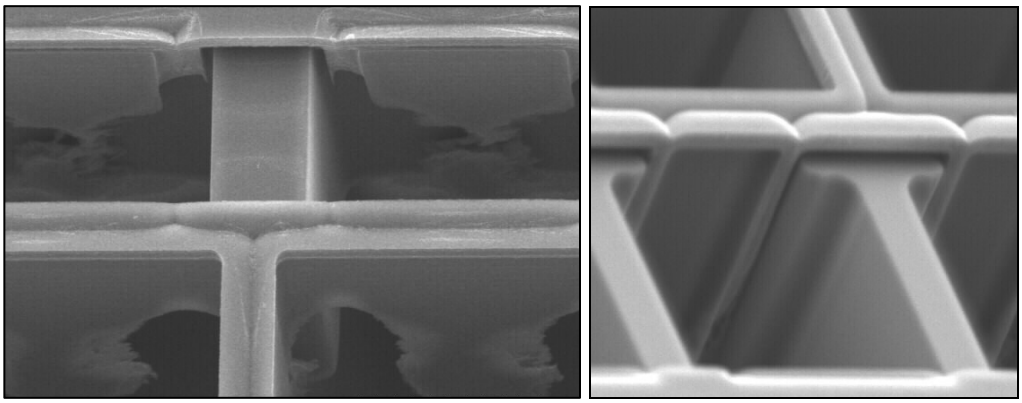


Figure 2.15. Buckling of a beam with aspect ratio of 100:1 (L=800 μm, W=8 μm) after growing 2 μm sacrificial oxide at 1000°C and release.

As mentioned in section 2.2, etching polysilicon inside the trench requires a sequence of high and low frequency plasma sources. The low frequency source is required to allow the long lifetime electrons to recombine with positive ions to neutralize the positive charge build up on the oxide sidewalls [94]. Figure 2.16.a shows the effect of high frequency source on over-etching the polysilicon electrodes. Figure 2.16.b is the polysilicon electrode etched using a sequence of high and low frequency sources. A final oxidation before releasing the dies can improve the surface roughness of the polysilicon electrodes.



(a) (b)

Figure 2.16. a) Effect of the high frequency source on over-etching the polysilicon electrodes, b) Polysilicon electrodes after proper combination of high and low frequency plasma sources.

2.4. Characterization of the HARPSS Accelerometer

The single side static sensitivity of the accelerometer is measured by applying a DC voltage, in the range of 0.1-1.1 V on a probe station, as depicted in Figure 2.17. The nonlinear rest capacitance change (ΔC) due to deflection (δd) is measured by a calibrated hp 4284A LCR meter. The drive voltage and capacitance change are related as in (2.22):

$$V_{DC} = (d_0 - \delta d)\sqrt{\frac{2K\delta d}{C_0 d_0}} = d_0\sqrt{\frac{2KC_0\Delta C}{(C_0 + \Delta C)^3}} \tag{2.22}$$

In order to find the equivalent acceleration that creates identical amount of deflection, for a certain actuation voltage, we use equation (2.23) and apply it into equation (2.22):

$$Ma = K\delta d \tag{2.23}$$

This will result in a nonlinear equation of (2.24) to correlate acceleration, a, DC voltage, V_{DC}, gap size, d_0, stiffness, K, and proof mass, M.

$$2Ma(d_0 - \frac{Ma}{K})^2 = C_0 d_0 V_{DC}^2 \tag{2.24}$$

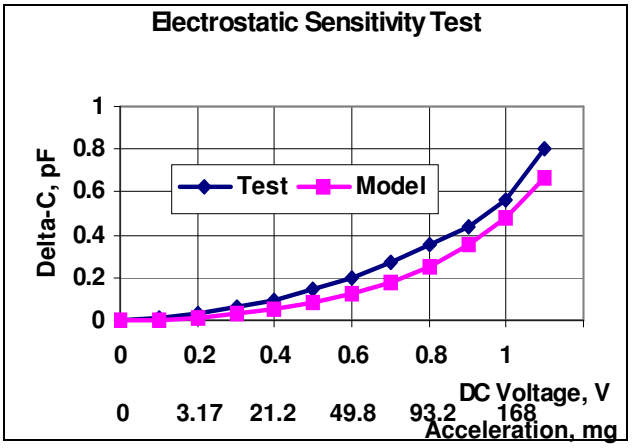


Figure 2.17. Electrostatic sensitivity test result of the 60 µm thick accelerometer [84].

Using equation (2.24), the equivalent gravity is plotted in Figure 2.17, leading to a sensitivity of 3.5 pF/g (at 1 g). The experimental results are slightly higher than modeling due to effect of non-equal gaps in the open loop system and oxidation-induced residual stress in SCS electrodes and springs.

The sensor was wire bonded to a switched capacitor interface circuit designed in 0.25 μm CMOS with a capacitance resolution of 3 aF/√Hz, the details of which are given in [71]. The circuit operates with a 2.5 V supply and has a differential voltage gain (*Vout/ΔC*) of 55 mV/pF and consumes a low power of 3 mW. Figure 2.18 shows the response of the system to static lateral accelerations in the range of 0-1 g. The offset is only 100 mV. The combined sensor and circuit sensitivity is measured to be 0.25 V/g, equivalent to a differential static sensitivity (*S*) of 4.5 pF/g that is close to the designed value (4.9 pF/g). This corresponds to *ENEA*=*MNEA*=0.67 μg/√Hz and *TNEA*=0.96 μg/√Hz [84]. The measured and estimated parameters of the HARPSS accelerometer are listed in Table 2.2. The proof mass of a broken accelerometer was measured using a milli-gram precision balance.

Table 2.2. Measured and calculated parameters of the 60 μm thick micro-g HARPSS accelerometer [84]

Measured parameter			**Calculated parameter**					
M *(mg)*	C_0 *(pF)*	*S* *(pF/g)*	*K* *(N/m)*	f_0 *(Hz)*	*BW* *(Hz)*	*D* *(Nm/s)*	*Q*	*TNEA* *(μg/√Hz)*
0.85	3.27	4.9	10.3	503	376	3.6×10^{-3}	0.8	0.96

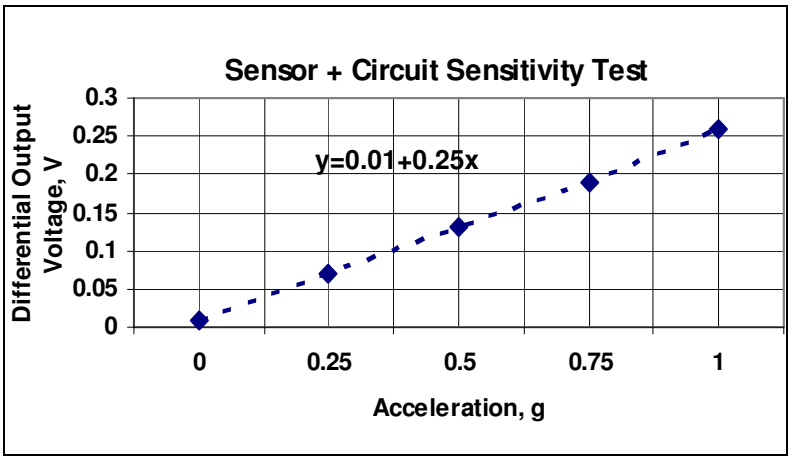


Figure 2.18. Measured electromechanical sensitivity vs. acceleration for the 60 µm thick HARPSS accelerometer [84].

2.5. Design and Analysis of the HARPSS in SOI Accelerometer

One main limit of the HARPSS in silicon accelerometer is the requirement for having release holes in the proof mass. In order to increase the density and increasing the mass, the most effective way is to eliminate these holes. In order to achieve this goal, the sensor can be made in SOI substrate. This way, the whole thickness of the device layer of an SOI wafer can be used as the proof mass, and the proof mass can be as thick as 400 µm. The handle wafer protects the sensor from backside and a proper packaging can protect it from the top. Using thick HARPSS-SOI process, sensors with smaller area can be fabricated, as compared to single-wafer HARPSS process.

A schematic of the HARPSS-on-SOI sensor is shown in Figure 2.19. The view of SCS mass, polysilicon electrodes, and nitride anchors is magnified in the same picture. The electrical isolation is provided by trench isolation. In this device, silicon nitride is not used to provide isolation, but is used to create self-aligned corrugations.

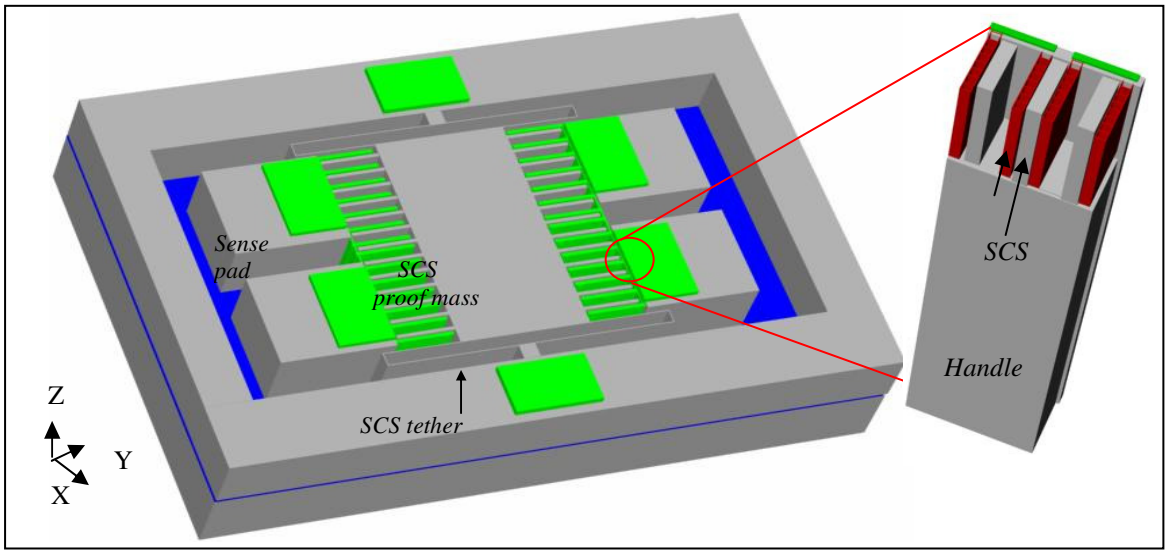


Figure 2.19. Schematic of the HARPSS-on-SOI accelerometer.

Modal simulation of a 150 µm thick sensor provides a first flexural mode (in-plane) of 227 Hz, as shown in Figure 2.20.a. The second and third modes (out of plane modes) are far away from the fundamental mode. The maximum detectable acceleration of the 150 µm sensor with an air gap of 1.5 µm (Δx<0.5 µm) is limited to $\omega_0^2 \Delta x$=100 mg. A limitation for such a heavy structure is its sensitivity to external shock excitations.

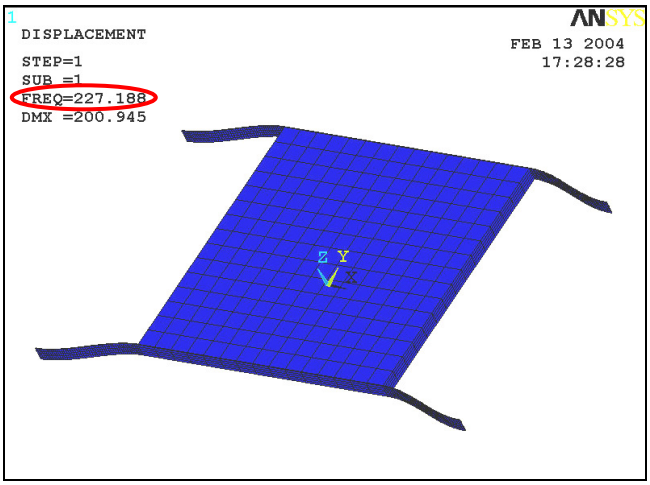
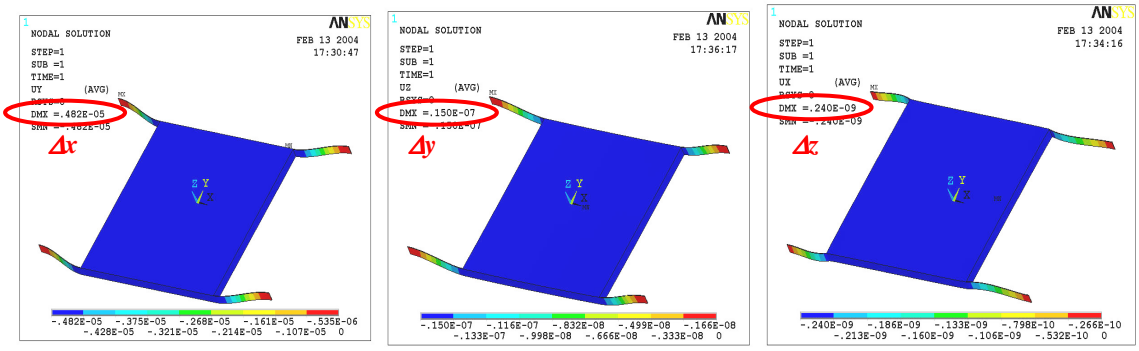


Figure 2.20. Simulation of fundamental resonance frequency of the 150 µm thick sensor.

Figure 2.21 shows the deflections (Δx, Δy, Δz) of the 150 µm thick sensor due to accelerations in the x, y, and z directions. The analysis provides an in-plane linearity ($k_X/k_Y=\Delta y/\Delta x$) of 0.3% and an off-plane linearity ($k_X/k_Z=\Delta z/\Delta x$) of 0.005%.



(a) (b) (c)

Figure 2.21. Static simulation of the 150 µm thick sensor for 1-g acceleration in (a) X direction, b) Y direction, c) Z direction.

The effect of environmental pressure on the HARPSS_SOI accelerometer noise floor is simulated and the results are shown in Figure 2.22. It is desirable to package the sensor before interfacing with the circuit to eliminate penetration of residues inside the gaps. This packaging can be done at atmosphere or vacuum pressure.

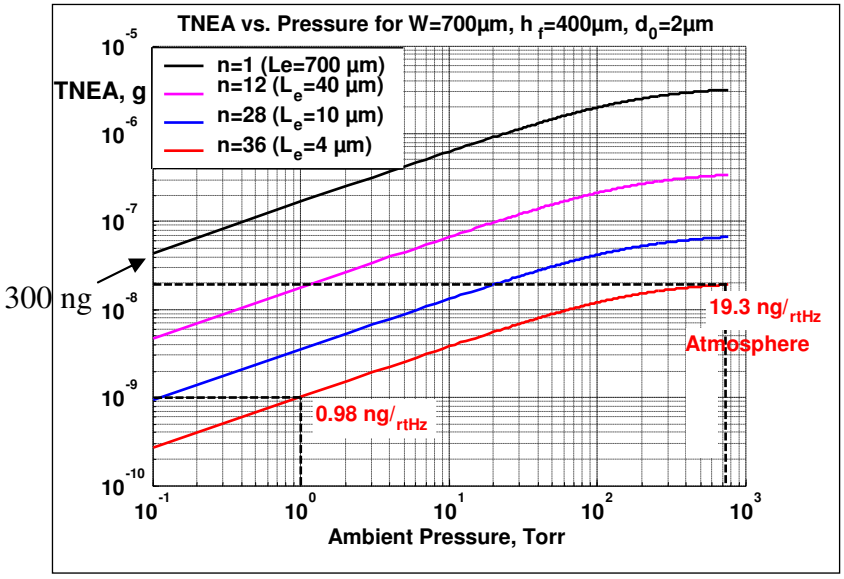


Figure 2.22. TNEA vs. pressure for a 400 µm thick device with a 2.0 µm gap and a 700 µm electrode.

A 400 μm thick non-corrugated (n=1) sensor with 700 μm long fingers (L_e=700 μm) operated in a vacuum level of 100 mTorr can have a theoretical mechanical noise floor of 300 ng/√Hz. Using n=36 corrugated electrodes can theoretically reduce the mechanical noise of the same sensor to 20 ng in atmosphere, eliminating the need for vacuum packaging. Non-vacuum encapsulation provides larger damping and smaller Q that is required for stable operation of the accelerometer.

2.6. Fabrication and Characterization of HARPSS-SOI Accelerometer

The process is very similar to regular HARPSS with the exception of the electrode corrugations being made using a self-aligned process. The HARPSS on SOI fabrication process flow, in particular the cross section of the electrode, mass and tether area, is depicted in Fig. 2.23. Starting with a thick, low resistivity SOI wafer, the nitride is deposited to define the anchors, corrugations and borders of the device. Structural trenches are defined by DRIE. This is followed by growing oxide as the sacrificial layer and trench-refill using thick LPCVD polysilicon. Next, polysilicon is etched at the surface and consequently, nitride is removed and the SCS will be etched in a DRIE tool to define the borders of the sensor and the corrugations. Then the back-side of the device will be aligned to the top-side and will be etched back, followed by etching the buried oxide. Finally, sacrificial oxide is removed in an HF/H_2O solution followed by super critical drying. To minimize stiction, the topside can be etched prior to the backside. Since the proof mass is still attached to the backside, no stiction will occur during HF release of the sacrificial oxide.

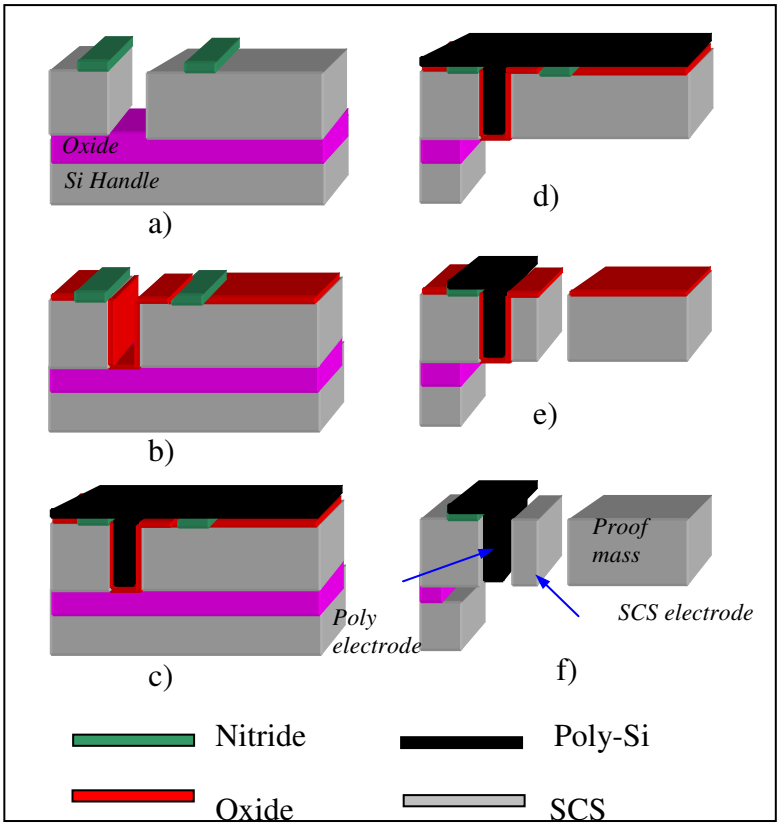
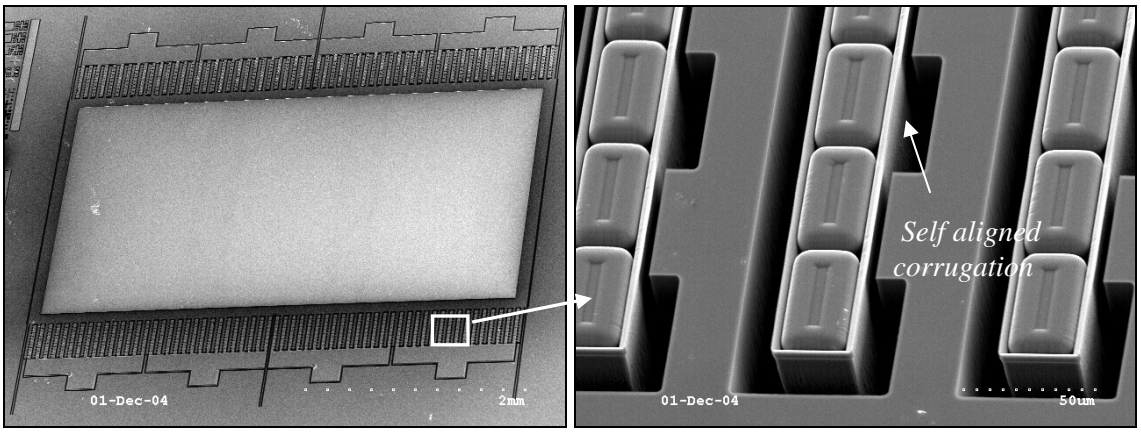


Figure 2.23. Process flow for the HARPSS on SOI accelerometer.

The trench profile is a function of the trench width. Wide silicon exposed areas are viable to grass type residues and conical etch profiles. We use a two step etching; one to realize the electrodes gaps (for sacrificial oxide definition) and one to define the accelerometer borders. Steps (a) to (d) are same as HARPSS-Si process. Finally, the backside of the sensor is patterned and etched, followed by HF release.

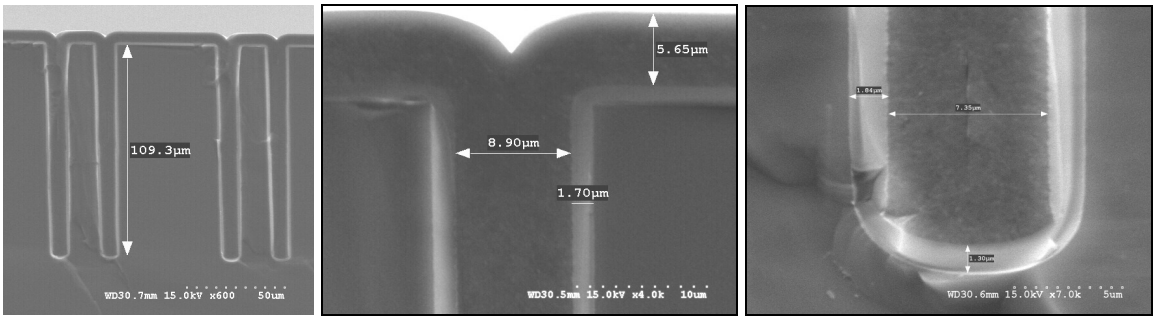
A 4 mm×2.8 mm HARPSS on SOI accelerometer was fabricated, and the SEM pictures are shown in Figure 2.24 for a 130 µm thick SOI wafer (device layer) with a 1.5 µm gap spacing defined by sacrificial thermal oxide.



(a) (b)

Figure 2.24. SEM View of a 130 µm thick HARPSS on SOI accelerometer.

The polysilicon electrodes are made by deposition of 5 µm thick LPCVD polysilicon, over the 1.5 µm thermal oxide, as shown in Figure 2.25.

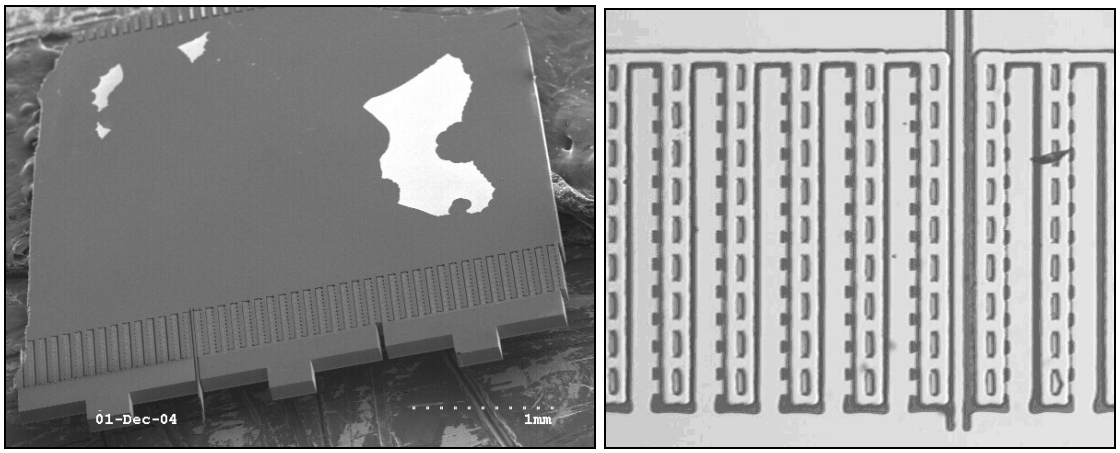


(a) (b) (c)

Fig. 2.25. (a) 110 µm deep trenches after trench-refill Top of the trench-refilled polysilicon, b) Top of the trench showing no void, c) Bottom of the trench.

In order to increase the rigidity and shock resistance of the polysilicon, the void should be minimized by etching trenches with positive profile (tapered), as shown in Figure 2.24.a.

Shown in Figure 2.26.a is the backside of the sensor after breaking it form the handle wafer and Figure 2.26.b shows that the electrodes and tethers are completely released.



(a) (b)

Fig. 2.26. SEM view of the backside of sensor: a) Overall view, b) Electrodes and tether.

As shown in Figure 2.27 for a 130 µm HARPSS-SOI accelerometer, the expected differential sensitivity is 50 pF/g for a 4mm×4.4mm sensor (M=5.4 mg) with a gap size of 2 µm, and 28 pF/g for a 4mm×2.8mm sensor (M=3.4 mg) with a gap size of 1.5 µm, respectively. The 4mm×2.8mm×130 µm device (Figure 2.24) was tested on a Suss PM5 probe station. As shown in Figure 2.28, the sensor shows a differential static sensitivity of 36 pF/V equivalent to 11.6 pF/g, which is about three times larger than the sensitivity of the 60 µm thick HARPSS sensor (Figure 2.18).

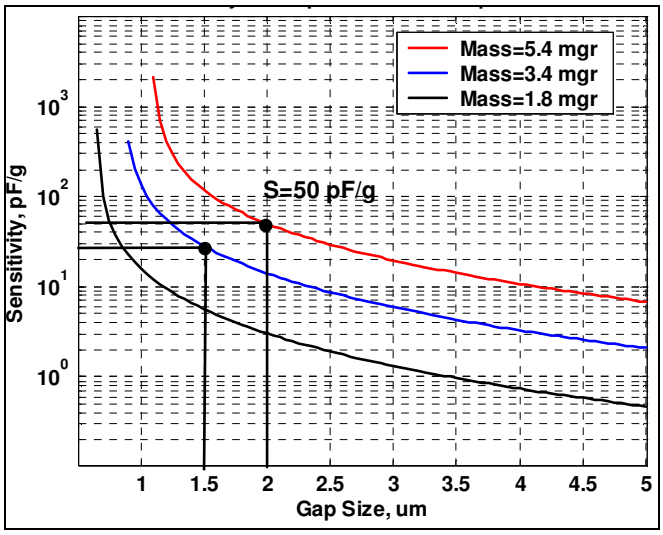


Figure 2.27. Modeled sensitivity of the HARPSS-SOI sensor.

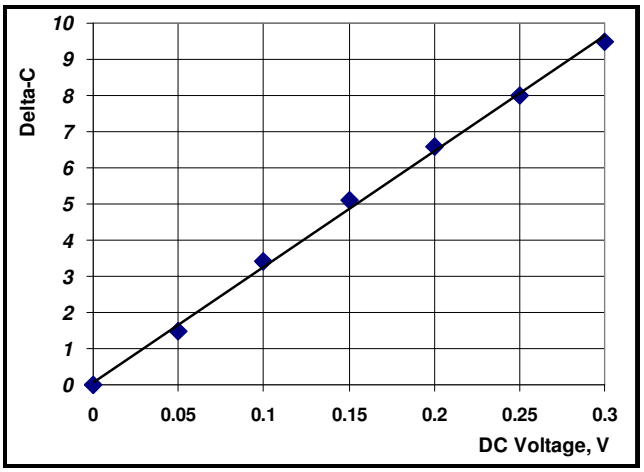


Figure 2.28. Electrostatic sensitivity test result of the 130 µm thick accelerometer.

Summary of the measured parameters of the HARPSS-SOI sensor are listed In Table 2.3. The expected TNEA of the sensor is about 350 ng/Hz.

Table 2.3. Measured and estimated parameters of the 130 µm thick HARPSS-SOI accelerometer.

Measured parameter			**Calculated parameter**			
M (mg)	*C_0 (pF)*	*S (pF/g)*	*K (N/m)*	*f_0 (Hz)*	*D (Nm/s)*	*TNEA (µg/√Hz)*
3.2	4.14	11.6	18.0	227	4.2×10^{-2}	0.35

Using the self-aligned HARPSS process, electrodes with a width of few micrometers can be fabricated, as shown in Figure 2.29. The corrugation width is only 3 µm, which is not possible to create using the original process.

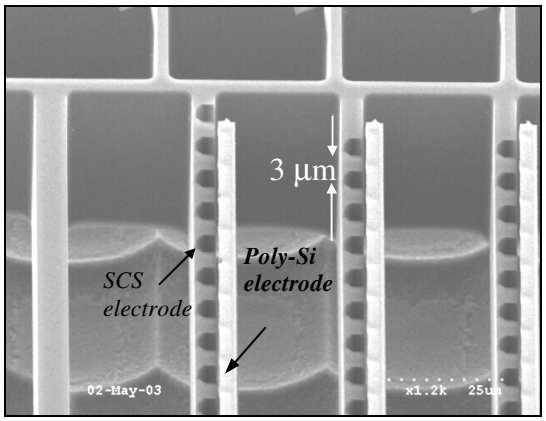


Figure 2.29. 3 µm wide corrugated electrodes made using the self-aligned HARPSS process [95].

2.7. Fabrication of High-Resolution Z-axis HARPSS Gyroscopes

The SCS HARPSS process was used to fabricate low-noise lateral tuning-fork gyroscopes. Figure 2.30 shows SEM view of a fabricated HARPSS tuning fork gyroscope [95]. The structure consists of a symmetrically supported double proof mass, a set of comb drive electrodes, a set of sense electrodes, and a set of tuning and quadrature error cancelling electrodes. The sensor is driven at resonance along the x-axis using comb-drive electrodes, and the rotation-induced Coriolis force is sensed along the y-axis. The symmetric double-mass architecture provides the differential sensing capability to reject the common mode accelerations or shocks.

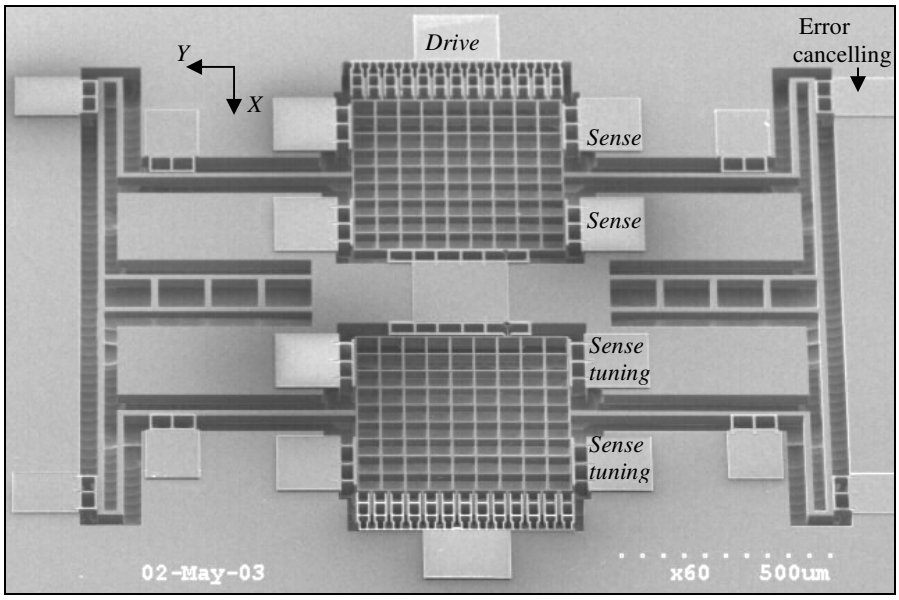
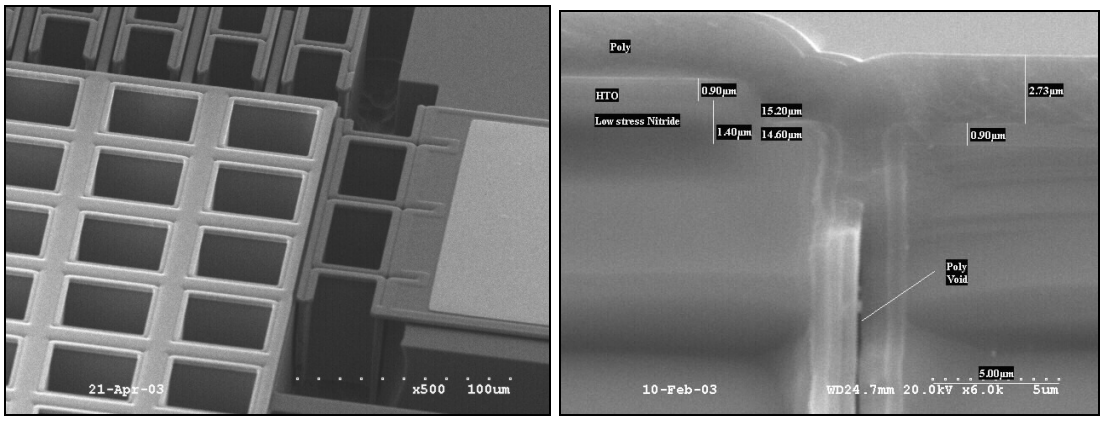


Figure 2.30. SEM view of a 70 μm thick HARPSS tuning-fork gyroscope with X/Y axis symmetry [95].

Due to high aspect ratio feature of the HARPSS process, the gaps can be reduced to sub-micron dimensions and the thickness of the actuator can be increased to more than 100 μm, to produce large drive forces (in the order of μN) using small drive and bias

voltages (<3 V) with comb-drive electrodes to increase the electromechanical coupling. The sensor thickness was 70 µm thick and the air gap was 0.75 µm, equivalent to an aspect ratio of 90:1. Exactly the same structure has been used in the ADI's polysilicon tuning fork gyroscope but with using a 20 times thinner structural layer (4 µm).

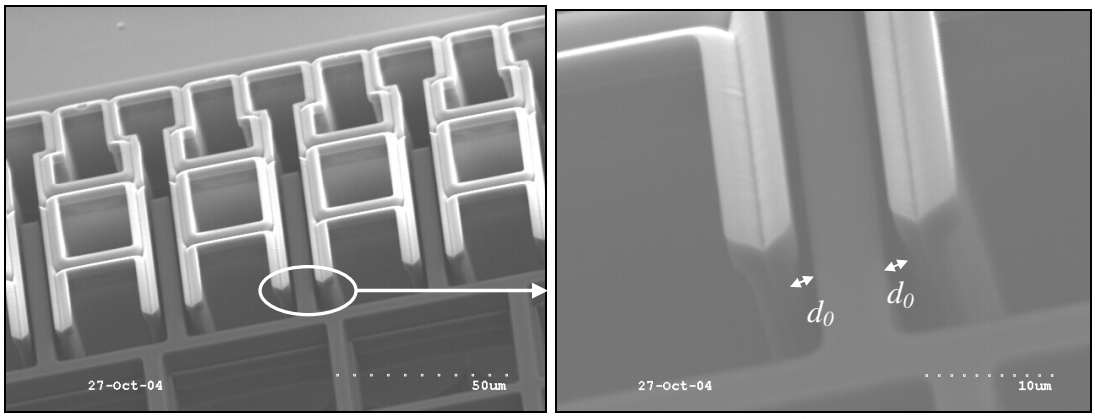
Figure 2.31.a and 2.31.b show close-up views of the sense electrode and the comb-drive fingers and the cross section of the anchor area.



(a) (b)

Figure 2.31. (a) SEM view of the mass and sense electrodes, b) Cross section of anchors using 1 µm thick HTO, 1.5 µm nitride, 0.75 µm thermal oxide as the gap, and 3 µm poly-Si [95].

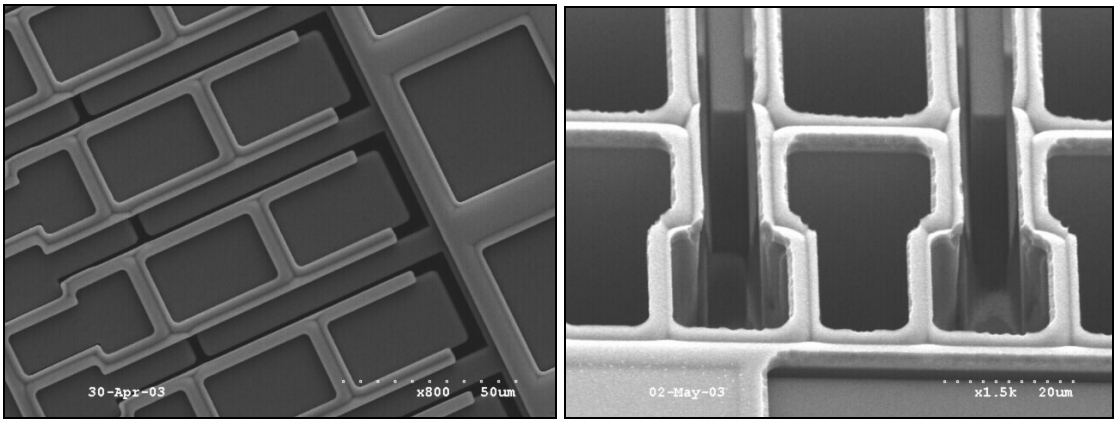
Figure 2.32 is a magnified view of the comb drive electrode with equal gap sizes to avoid lateral snap down, which requires a perfect lithography alignment.



(a) (b)

Figure 2.32. (a) SEM micrograph of the proof mass and drive electrodes, b) Magnified view of the comb drive electrodes, looking from the proof mass.

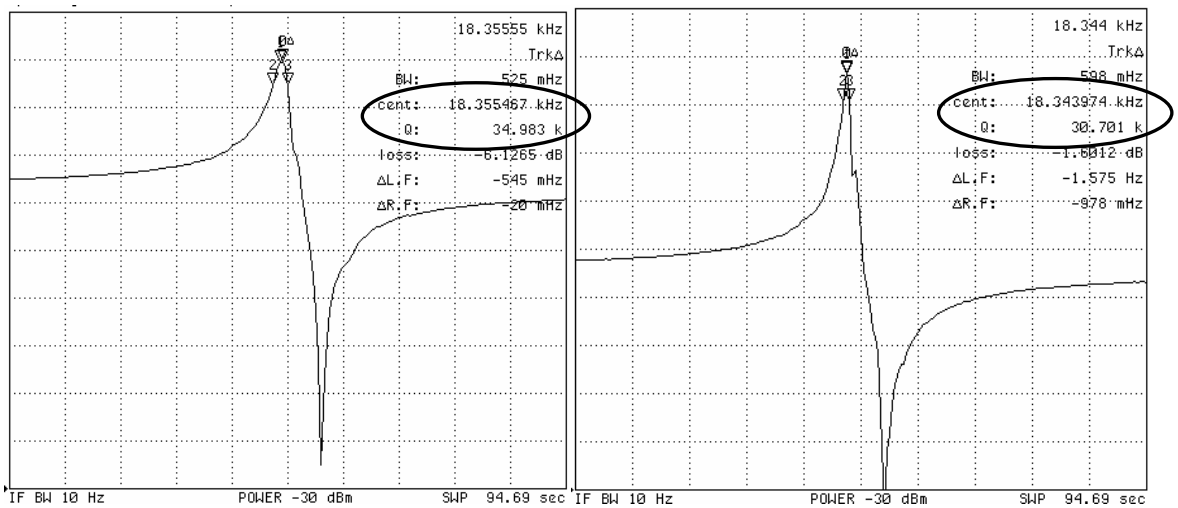
The micrograph of the polysilicon electrodes right after the polysilicon etching step is shown in Figure 2.33.a. The SCS island will be etched during isotropic release step. Figure 2.33.b shows the magnified view of the drive electrodes looking from the anchor area. The extra SCS island has been completely removed.



(a) (b)

Figure 2.33. (a) SEM micrograph of the comb drive electrodes right after polysilicon etching, b) View of the comb drive electrodes from the anchor area.

The gyroscopes were wire-bonded onto a PCB with up to four OP656 amplifier channels used in a trans-impedance amplifying configuration to amplify the sense current. The DC polarization voltage (V_P) was in the range of 2-3 V, and the comb drive AC voltage (V_D) was -30 dBm. The two first resonance modes of the device show a closely spaced resonance frequencies at 18.34 kHz and 18.35 kHz with a quality factor of ~30,000 in a vacuum level of 10^{-4} Torr, as depicted in Figure 2.34. The Q of the sense mode is slightly lower than that of the drive mode, due to possible moments in the sense direction. The sense mode is 12 Hz higher than the drive mode, the sense-tuning electrodes can be used to lower the sense mode frequency and match the two flexural modes.



(a) (b)

Figure 2.34. (a) Measured drive mode resonant *Q*, (b) Measured sense mode resonant Q using V_P=2V, V_D= -30dBm [95].

The Brownian noise floor of the tuning fork gyroscope is evaluated as the following:

$$\Omega_{z(Brownian)} = \frac{1}{2x_d}\sqrt{\frac{4k_BT}{\omega_0 MQ}}\sqrt{BW} \tag{2.25}$$

Here x_d indicates the drive amplitude, k_B is the Boltzmann's constant, T is the absolute temperature, ω_0 is the resonant drive frequency, M is the effective mass in the sense direction, Q is the quality factor, and BW is the measurement bandwidth. HARPSS tuning fork gyroscope provides large mass, high-Q operation, large drive amplitudes, and large sense capacitances. Equation (2.25) suggests that the Brownian noise floor of the HARPSS tuning fork gyroscope with large drive amplitude (x_d>1 μm) and enough mass (M>0.5 mg) is below 1 °/hr/√Hz.

As is the case for the tunable capacitor and accelerometer, the gyroscope needs a low voltage operation of only 2 V because of the high aspect ratio nature of the device (large drive/sense capacitance).

CHAPTER III

DESIGN AND FABRICATION OF HARPSS VARACTORS

This chapter covers the design of the parallel plate (gap-adjustable) in-plane HARPSS varactors utilizing electrostatic actuation. The varactors are aimed for tunable filters and phase shifters in L and C bands with low actuation voltages, as listed in Table 3.1. In all designs, the ground plate is movable and the capacitor and actuator plates are fixed.

Table 3.1. Design specifications for the designed low-voltage tunable capacitors

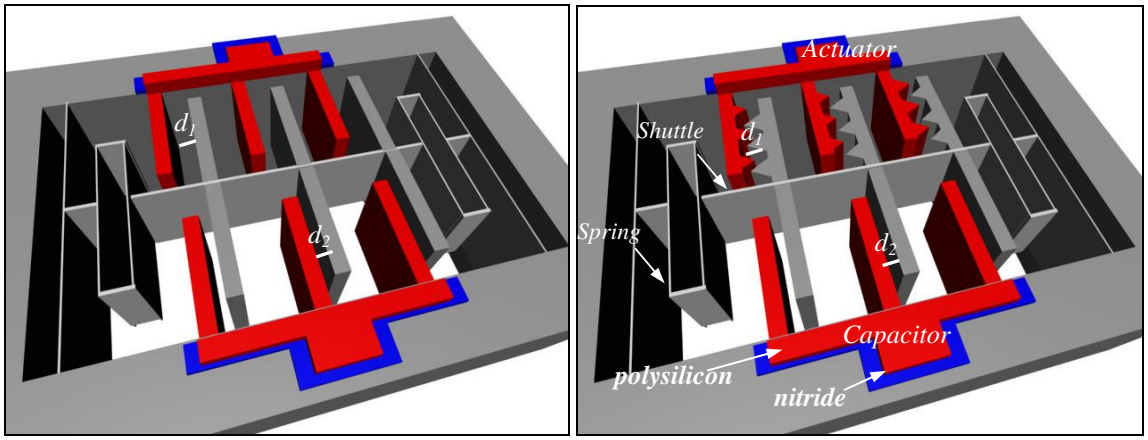
Type	Tuning range	Q at 1 GHz	Q at 5 GHz	Unique feature
HARPSS	>2:1 at 2 V	>50	>10	Smallest size

3.1. Design of HARPSS Varactors

The schematic of the proposed one-port HARPSS varactor is shown in Figure 3.1. The ground plane is the movable shuttle anchored at four or two corners. The two sections of spring are attached in the middle junction to avoid rotation during actuation. The meander-shape design of the tethers provides lowers the tuning voltages and also reduces the series inductance. The capacitor and actuator have different gap sizes to provide a non-pull-in limited tuning. Assuming d_1 is the tuning gap size, and d_2 is the capacitor gap size, then the ideal tuning range of the varactor can be expressed as in (3.1):

$$\frac{\Delta C}{C}(\max) = \frac{\frac{\varepsilon_0 A}{d_2} - \frac{\varepsilon_0 A}{d_{\max}}}{\frac{\varepsilon_0 A}{d_2}} = \frac{\frac{\varepsilon_0 A}{d_2} - \frac{\varepsilon_0 A}{(d_1/3)}}{\frac{\varepsilon_0 A}{d_2}} = \frac{1}{1 - \frac{d_1}{3 d_2}} \tag{3.1}$$

To increase the tuning range, it is necessary to have the actuation displacement larger than the capacitor displacement (d_1>d_2). In the special case, where d_1=3d_2, a theoretical tuning range of infinity is expected. However, the dual gap design (Figure 3.1.a) requires complication in the bulk fabrication process. One gap can be defined with a sacrificial oxide and the other gap by DRIE. Another solution to create double gap is to use a zig-zag shape (Figure 3.1.b) in the actuator to enable larger effective travel range for the actuator plate, as opposed to the capacitor plate.



(a) (b)

Figure 3.1. Schematics of the HARPSS varactor: a) Dual gap tuning, b) Zig-zag tuning [96].

The HARPSS varactors of Figure 3.1 have a complicated distributed circuit model, consisting of capacitors, resistors, and inductors. Figure 3.2 shows a simplified lumped model by integrating all the poly-Si/SCS capacitors into C, and all and series resistors into R_S, all the inductors into L, and the dielectric parasitics into C_P and R_P.

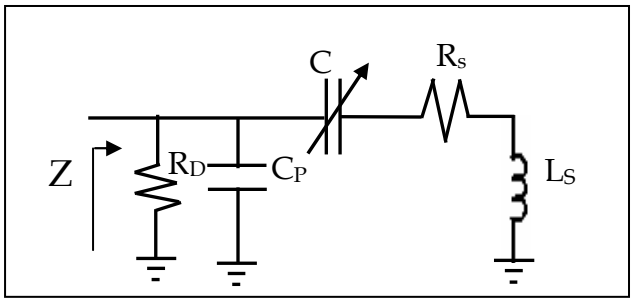


Figure 3.2. Electrical model of the one-port HARPSS varactor [97].

A proper design dictates C_P<<$C(min)$, R_P>> $C_P\omega$. Using low-loss dielectric results in an extra large R_P. For an isotropic dielectric, R_P and C_P will be related as in 3.2:

$$R_P(f) = \frac{1}{C_P(f)} \frac{\varepsilon(f)}{\sigma(f)} \tag{3.2}$$

For oxide as the dielectric, ε=66pF/m^2, σ=10^{-12} S/m. Assuming C_P=0.4 pF at 1GHz, then equation (3.2) gives R_P=1.66 TΩ at 1 GHz, which is much larger than $C_P\omega$ (=400 Ω), therefore R_P can be removed from the electrical model. The equivalent Q factor for the frequencies below Self Resonance Frequency, SRF, is simplified as in (3.3):

$$Q(\omega) = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} = \frac{C_P + C - C(2LC_P - R^2C^2C_P)\omega^2 + L^2C^2C_P\omega^4}{(2C_P + C)RC\omega - RLC^2C_P\omega^3} \tag{3.3}$$

At low frequencies, assuming C_P<<C, Q can be estimated as the following:

$$Q(\omega \to DC) \cong \frac{(C_P + C)}{(2C_P + C)RC\omega} \cong \frac{1}{RC\omega} \tag{3.4}$$

At high frequencies below SRF, $LC\omega^2$<<1. If 2L>>R^2C, the Q factor can be simplified as:

$$Q(DC << \omega < SRF) \cong \frac{-C(2LC_P - R^2C^2C_P)\omega^2}{-RLC^2C_P\omega^3} \cong \frac{2}{RC\omega} = \frac{3}{4\pi fC\rho \dfrac{L_{spring}}{HW_{Spring}}} \tag{3.5}$$

The zig-zag tuning scheme can be modeled by coupled-mode multiphysics analysis in ANSYS. One alternate method is to find the rest capacitance at zero bias, by applying

a 1V voltage difference to electrodes, find the local surface charges, and then use (3.5) to find the total charge, Q, on all surfaces along each segment (l_i), t is the capacitor height, V is the voltage difference, d_0 is the gap, and θ is the tilt angle:

$$C = \frac{Q}{V} = \frac{t\sum_i \rho_{S,i} d_{S,i}}{V} = \frac{t\dfrac{d_0}{\cos\theta}\sum_i \rho_{S,i} l_i}{V} \tag{3.6}$$

Figure 3.3 shows the FEMLAB analysis to derive the total charge and rest capacitance of the zig-zag structure, accounting for fringing fields. Shown in the figure is the magnitude of the surface electric field, which is maximized at the sharp corners.

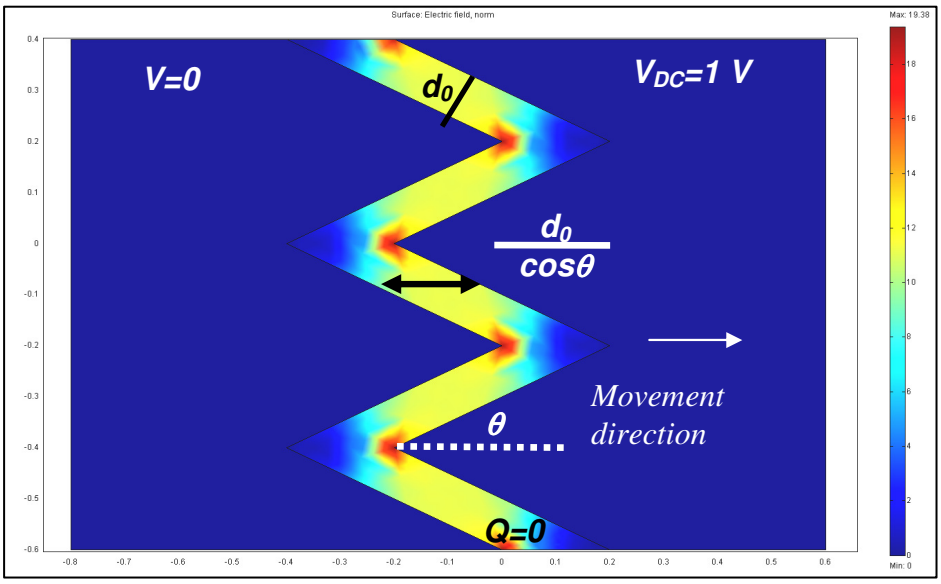


Figure 3.3. FEMLAB analysis of the DC electric field inside the air gap in the zig-zag electrodes.

After finding the rest capacitance, the non-linear voltage dependent capacitance change can be derived from for small deflections, as in (3.7):

$$V_{DC} = d_0\sqrt{\frac{2KC_0\Delta C}{(C_0+\Delta C)^3}}, \qquad \Delta C(x << d_0) \cong \frac{C_0^2}{2K}V_{DC}^2 \tag{3.7}$$

The mentioned approximation can be used up to x<0.25d_0 with an error of better than 40%. This approach will significantly reduce the complexity of the analysis to model the

electrostatic operation of the varactor and can be also applied to other capacitive devices.

The pull-in voltage of the actuator is strongly dependent on the average air gap and the aspect ratio of the tethers, and is independent of the device height, as in (3.8).

$$V_{pull-in} = \sqrt{\frac{8K(\frac{d_{Ox}}{\cos\theta})^3}{27\varepsilon_0 HNL_{Actuator}}}) \tag{3.8}$$

K is the spring constant, E is the SCS Young's modulus (159 GPa for (100)), d_{0x} is the average air gap at zero-bias, ε_0 is the air permitivity, H is the electrode height, and $L_{Actuator}$ is the total length of the capacitor (3.6 mm). For a gap of 1 μm, the theoretical value of $V_{pull-in}$ for the actuator is 4.5 V, and the measured $V_{pull-in}$ is 4 V. If the pad capacitance is much smaller than the device capacitance ($A_{pad} << A_{cap}$), the maximum tuning range can be expressed as in equation (3.9) (θ=65° is the slant angle, as in Figure 3.3) [96]. For d_{Ox}=1μm, the maximum tuning range of the capacitor is 3:1.

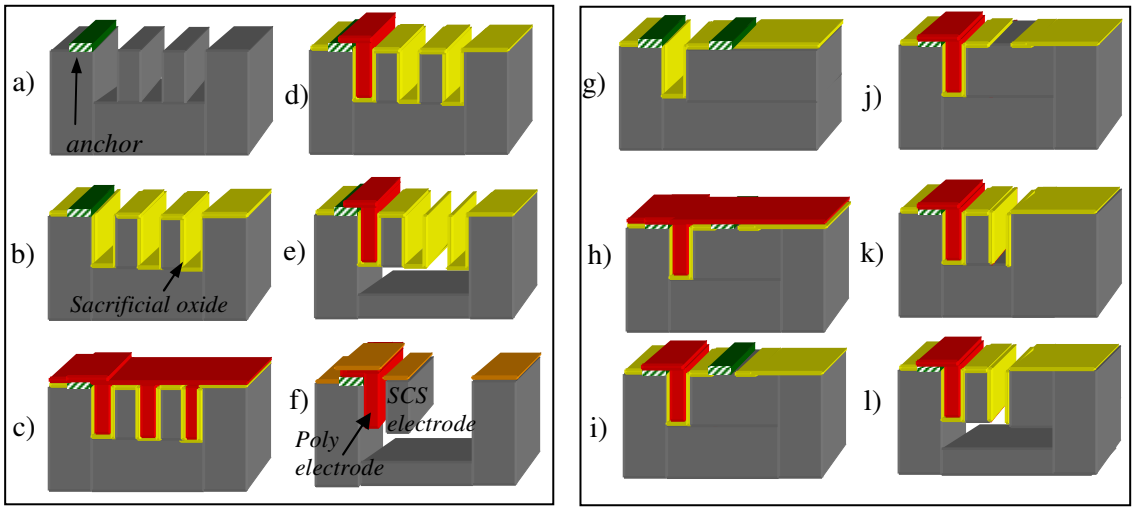
$$\frac{\Delta C}{C_0}(\max) \cong \frac{\Delta C}{C_{cap}} = \frac{\Delta d}{d_{Ox} - \Delta d} = \frac{\frac{d_{Ox}}{3\cos\theta}}{d_{Ox} - \frac{d_{Ox}}{3\cos\theta}} = \frac{1}{3\cos\theta - 1} \tag{3.9}$$

3.2. HARPSS Process Design for RF MEMS

Two HARPSS methods are presented. The regular sequence (Figure 3.4.left) starts with patterning the low-stress nitride (Appendix C), followed by defining the trench (Figure 3.4.a). A thin layer of sacrificial oxide is grown to uniformly cover the trench sidewalls and define the high aspect ratio capacitive gap (Figure 3.4.b). Trenches are refilled with doped polysilicon (Figure 3.4.c). The polysilicon will be removed from the surface and inside the isolation trenches around the electrodes [92] (Figure 3.4.d). The device is released in a DRIE tool (Figure 3.4.e), followed by removing the oxide in HF.

Finally a layer of metal is evaporated to reduce the series resistance (Figure 3.4.f). The metal thickness is less than the insulator thickness. The pad can be fabricated on top of thick oxide islands to further reduce the pad capacitance and integrate high-Q inductors on the same die. The silicon substrate has been over-etched to minimize the substrate loss.

The self-aligned sequence (Figure 3.4.right) starts with patterning the low-stress nitride, defining the trench and growing oxide (Figure 3.4.g). Trenches are refilled with doped polysilicon (Figure 3.4.h). The polysilicon will be removed only from the surface [92] (Figure 3.4.i). A thin layer of oxide is grown on polysilicon, then the nitride that is not covered with polysilicon is removed in phosphoric acid (Figure 3.4.j). The silicon under the nitride openings is then etched in a DRIE tool, followed by deposition of LPCVD oxide and removing the oxide from bottom of the trench in an ICP. (Figure 3.4.k). Finally an isotropic etch releases the electrodes, followed by final HF release. A layer of metal is evaporated to reduce the series resistance. The self-aligned process can provide narrower electrodes but requires more number of furnace runs.



(left) (right)

Figure 3.4. left) 4-mask HARPSS process flow, right) 3-mask self-aligned HARPSS process flow.

3.3. HARPSS Varactor Modeling

The HARPSS varactor has been modeled in Ansoft™ HFSS electromagnetic field solver to study the RF loss and electrical *Q* factor for the complicated 3-D structure. To ensure that radiation boundary conditions are set up properly, instead of defining air radiation boundary around the structure, a set of Perfectly Matched Layers (PML) boundaries have been defined to enable radiation surfaces to be located closer to radiating objects. Figure 3.5 shows different PML as free space termination boundaries with zero reflection at the PML/air interface in HFSS. Because of three dimensional identity of the HARPSS process, other solvers such as Sonnet™ and ADS momentum can not accurately model the HARPSS varactor. The structure is placed on a ground from bottom and an infinitely large air box from the top. The RF excitation in the range of 0.1 GHz to 10 GHz has been applied in a Coplanar Waveguide (CPW) configuration to the pad.

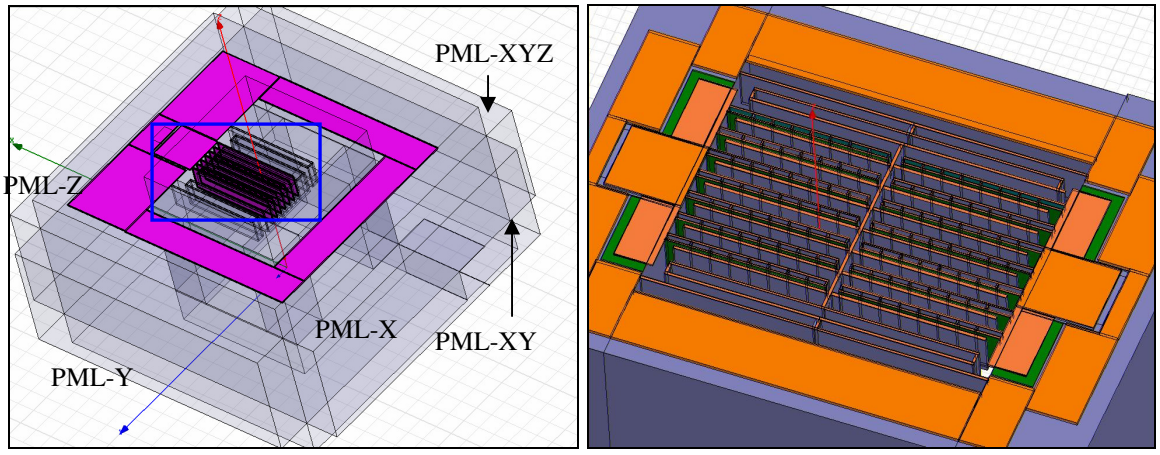
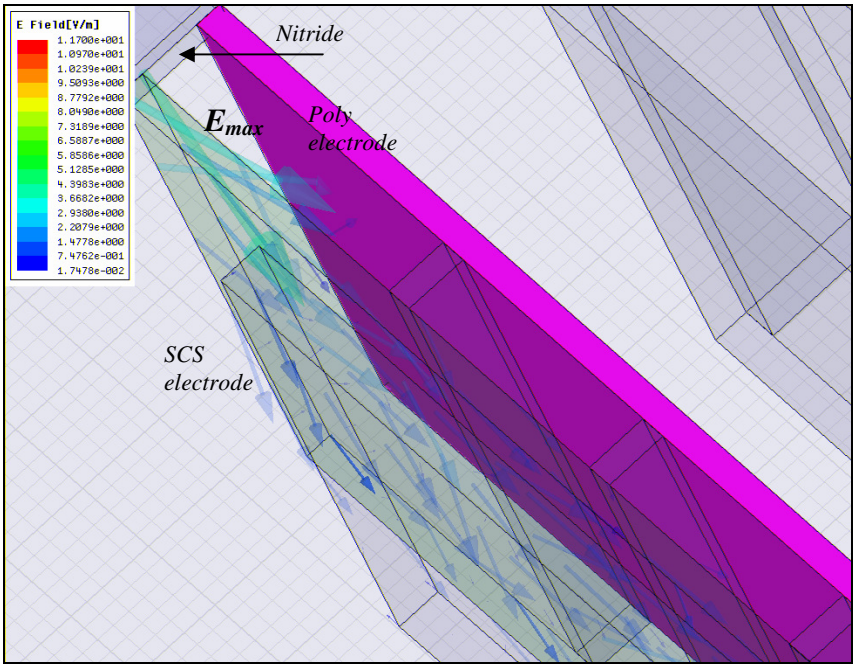


Figure 3.5. a) The HARPSS varactor and the PML boundaries, b) Close up view of the polysilicon fixed electrodes and silicon movable electrodes/tethers [97].

Figure 3.6 shows the electrostatic simulation results for a HARPSS device having 2 µm thick low stress nitride, 3 µm thick polysilicon, 60 µm thick SCS structure, and a 1

µm gold overcoat. As shown in Figure 3.6.a, the magnitude of the electrostatic field at 1 GHz is at maximum (E_{max}) at the top polysilicon junction close to the nitride anchors.

(a)



(b)

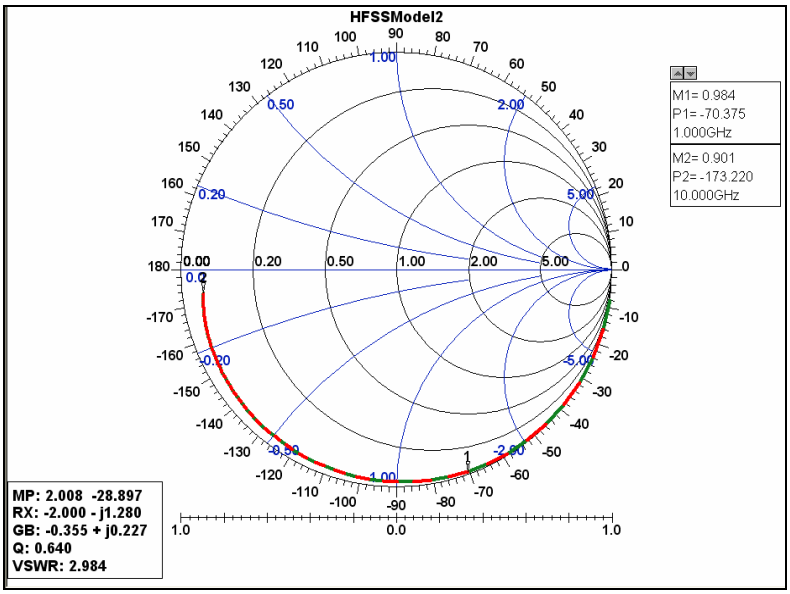
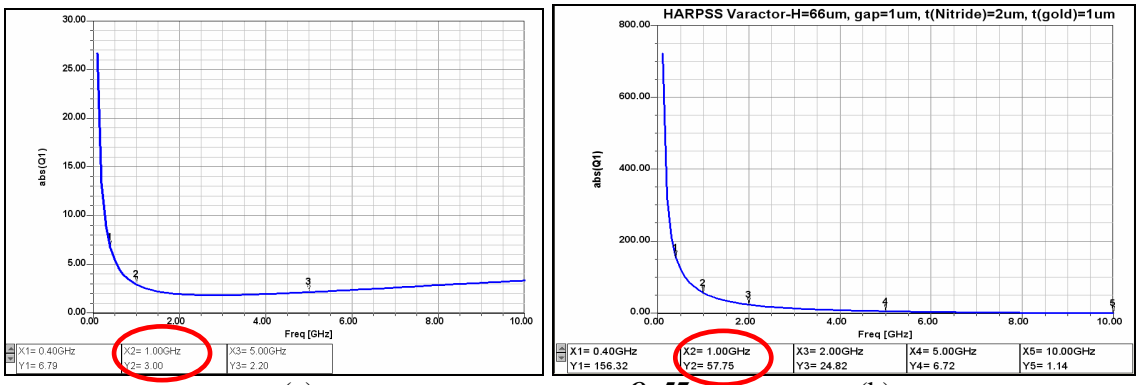


Figure 3.6. a) Vector plot of the electric field between polysilicon and SCS electrodes in HFSS, b) Smith chart of the return loss for the one-port varactor in the frequency range of 0.5-10 GHz

Figure 3.6.b shows the simulated return loss in the 0.5-10 GHz; proving that the SRF is above 10 GHz. The meander design of the SCS tether has decreased the series inductance to extend the SRF to above 10 GHz. As shown in Figure 3.7, the gold

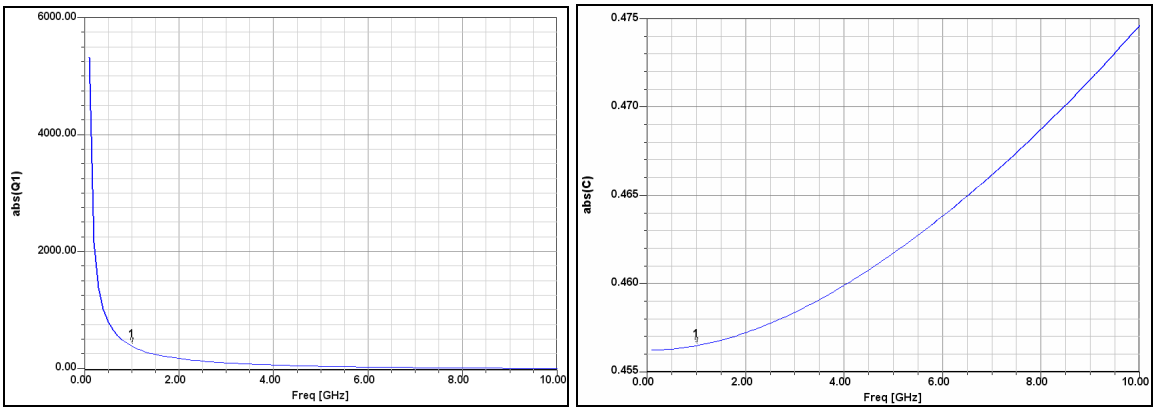
overcoat has a significant impact on increasing the *Q*-factor; while SCS structure provides a *Q* of 3 at 1 GHz, a 1 µm gold overcoat increases the *Q*-factor to 57 at 1 GHz.



Q=3 (a) *Q=57* (b)

Figure 3.7. Simulation of *Q* factor in HFSS: (a) *Q* for the 60 µm thick HARPSS varactor before gold evaporation; (b) *Q* for the same SCS structure utilizing 1 µm gold overcoat.

The *Q* factor was evaluated as the ratio of the imaginary part to the real part of the input admittance. In order to study the electrical properties of the HARPSS anchor, the pad capacitance was modeled. As Figure 3.8 shows, *Q* factor of the pad capacitance is about 400 at 1 GHz, proving that the pad electrical loss is smaller than the device itself.

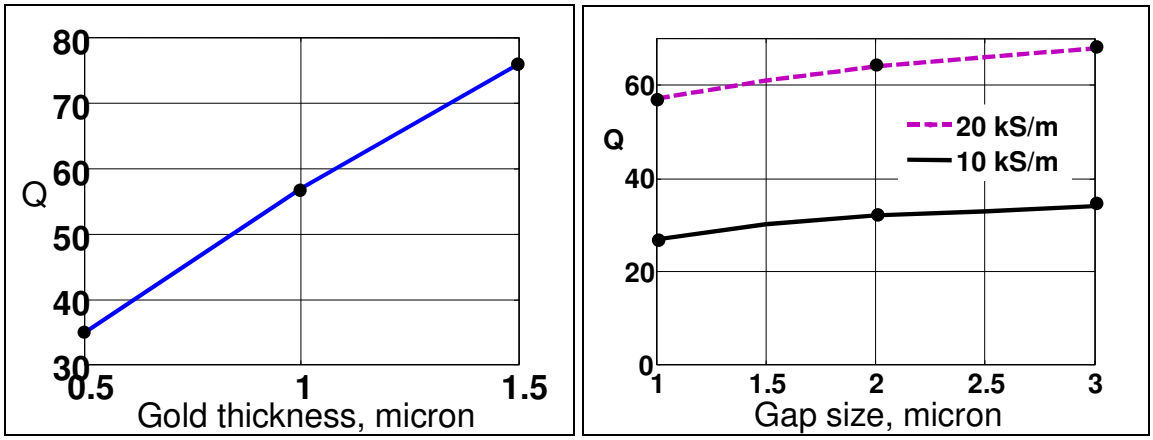


(a) (b)

Figure 3.8. HFSS simulation of the HARPSS pad capacitance (a) *Q* factor, b) Capacitance value.

Since the pad capacitance is much smaller than the device capacitance, therefore de-embedding the pad capacitance does not improve the *Q* factor significantly.

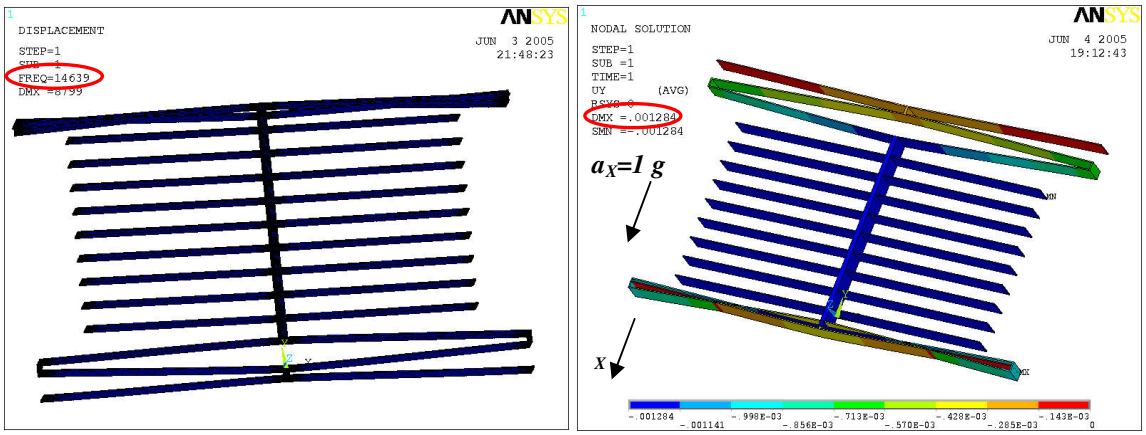
Measurement of the Q-factor for metal thicknesses in the range of 1-3 µm and gap sizes from 0.5-1.5 µm is shown in Figure 3.9, proving that Q is a strong function of the gold thickness and the silicon bulk conductivity, but a weak function of the air gap.



(a) (b)

Figure 3.9. Measured Q factor of the 1 pF HARPSS varactor: a) For different gold thickness, b) For different gap sizes [97].

The modal simulation of the HARPSS capacitor in ANSYS^{TM} shows a resonant mode at 14 kHz, therefore the tuning frequency range is DC-14 kHz. The mechanical stability of the varactor is analyzed by applying 1 g in-plane acceleration, as shown in Figure 3.10. For d_0=1 µm and C=1 pF, the acceleration sensitivity is only 1 fF/g.



(a) (b)

Figure 3.10. a) Modal analysis, b) Static deflection due to 1 g lateral acceleration [97].

3.4. Implementation and DC/RF Characterization of the HARPSS Varactor

All three types of MEMS varactors have been fabricated and tested. Figure 3.11 shows the SEM view of a 60 µm thick HARPSS varactor with 1.5 µm gaps equivalent to an aspect of 60:1 [96]. The device occupies an area of 1.6 mm×1 mm=1.6 mm^2 area. The design has been improved to make use of HARPSS small size capabilities, and as shown in Figure 3.12, almost same amount of capacitance can be obtained with 75% of reduction in area by using the self-aligned process. The dual-gap device occupies only 0.65 mm×0.65 mm=0.42 mm^2.

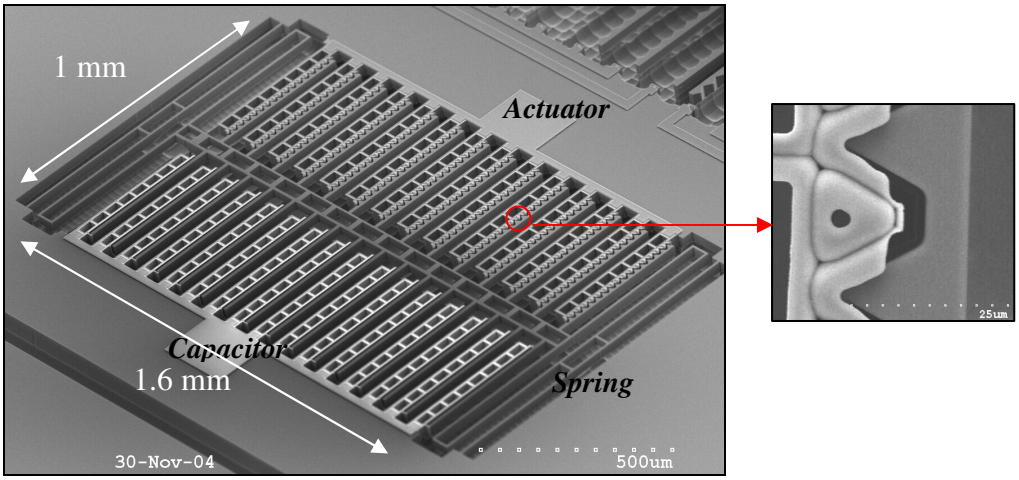


Figure 3.11. SEM view of a 60 µm thick HARPSS zig-zag varactor [96].

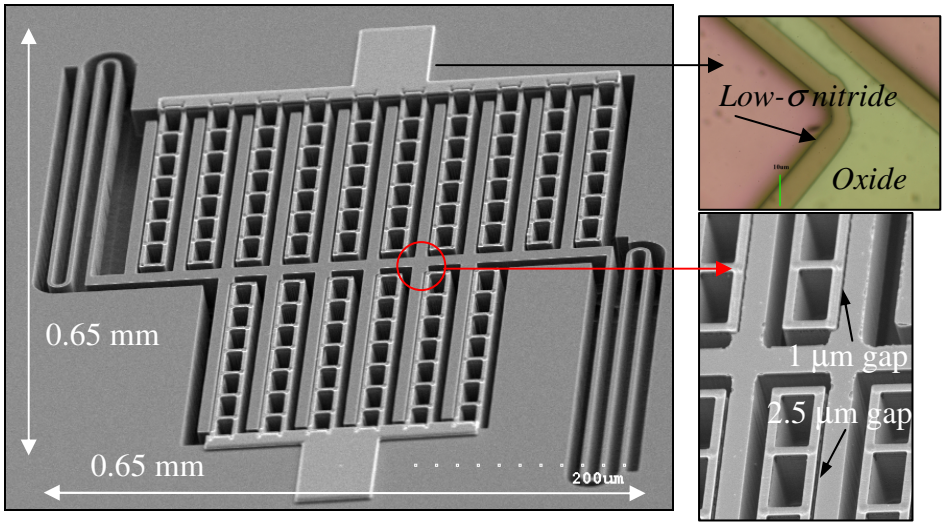
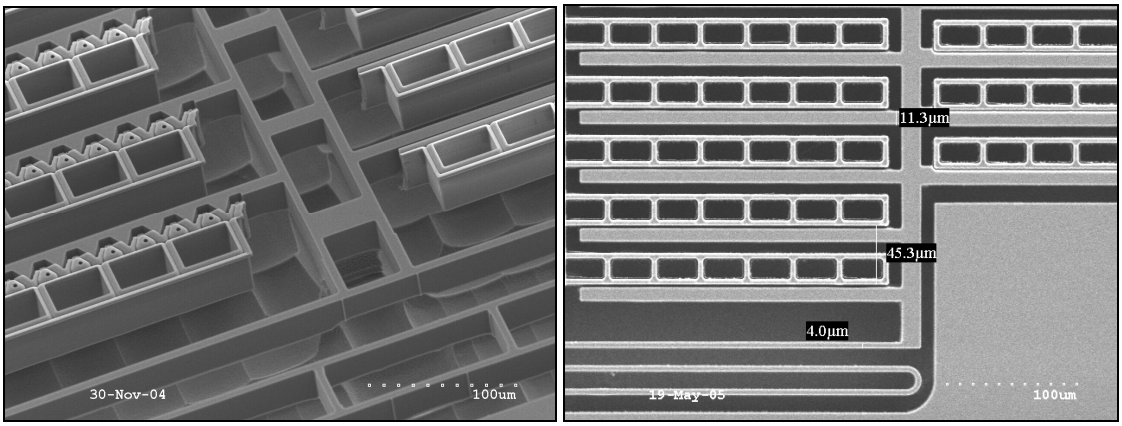


Figure 3.12. SEM view of a fabricated HARPSS dual gap varactor [97].

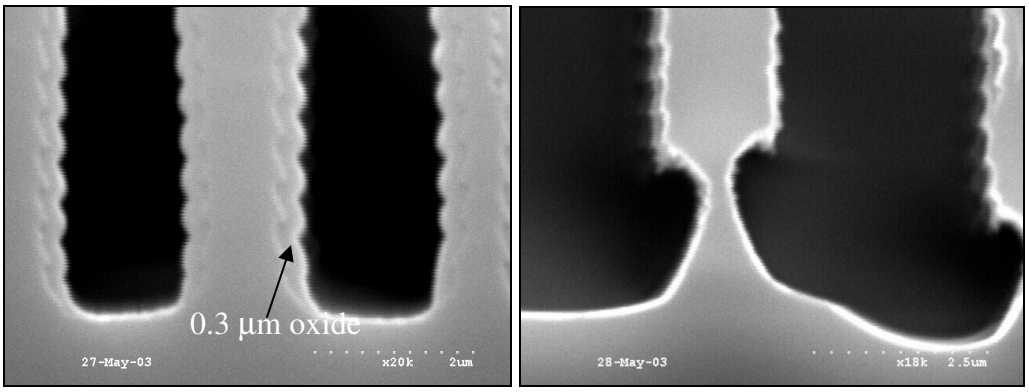
No release holes have been designed in the SCS shuttle or electrodes and this ends to decrease the size significantly. The only disadvantage in the dual-gap device is that the gap could not be defined as precise as the zig-zag design. The close up view of the meander SCS tethers, SCS shuttle, poly-Si/SCS tuning and capacitor electrodes for the HARPSS varactor of Figure 3.11 is magnified in Figure 3.13.a. This figure clearly shows that by over-etching the substrate under the electrodes, the substrate parasitics can be reduced significantly, a feature that is not present with the SOI device. Here, the average gap in the tuning side is about two times the average gap in the capacitor side. The view of the dual-gap HARPSS varactor of Figure 3.12 is shown in Figure 3.13.b. The dual-gap design has an electrode pitch of 45 μm that is less than half of the previous version (93 μm). The capacitor gap is created using the sacrificial oxide, and the tuning gap is created using the self-aligned method.



(a) (b)

Figure 3.13. Close-up view of the HARPSS varactors: a) Zig-zag design, b) Dual-gap design.

The release step in the self aligned method is highlighted in Figure 3.14. Figure 3.14.a shows the silicon beam after deposition and dry etching of LPCVD oxide (step k in Figure 3.4). Figure 3.1.4b is the same after releasing the beam (step l in Figure 3.4).



(a) (b)

Figure 3.14. a) View of the SCS beam after depositing LPCVD oxide, b) After isotropic release.

As shown in Figure 3.15, the HARPSS varactor of Figure 3.13 shows a wide tuning ratio of near 2:1 over a 3-6 pF range, measured using a calibrated hp4284A LCR meter after applying 2V to the actuator on a probe station [96]. The DC test result is slightly higher than model, and this is because of the fact that HARPSS silicon device has inherent compressive stress that can cause the stiffness to be different from the theory.

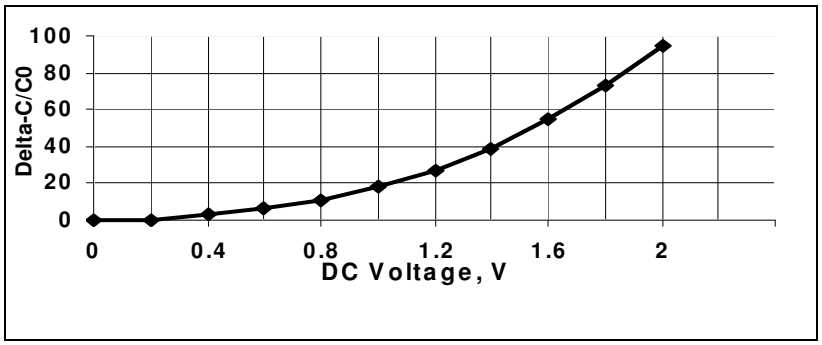
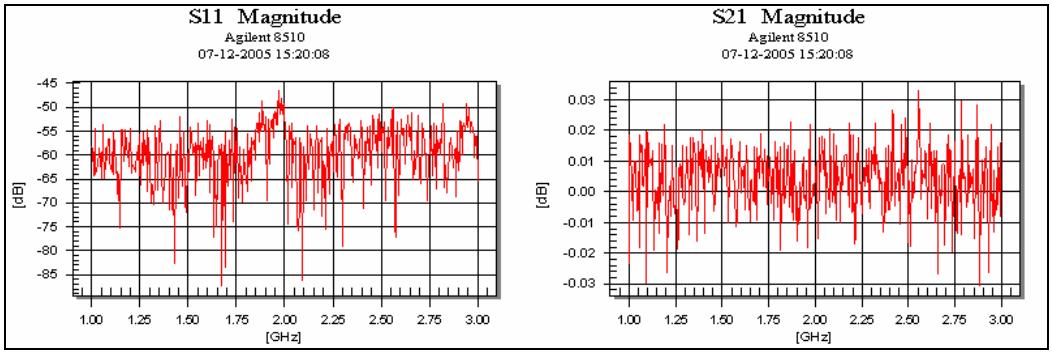


Figure 3.15. Measured tuning range of the 60 µm thick HARPSS varactor with 1 µm air gap [96].

The RF performance of the HARPSS varactor was measured with an Agilent-8510 vector network analyzer and an RF probe station in a two-port configuration. Cascade GSG microwave probes with a 150 µm pitch were used for measurements. An SOLT calibration was performed. Since the MEMS device is very linear, a maximum RF power of 10 dBm can be used. Figure 3.16 shows the through return and insertion loss

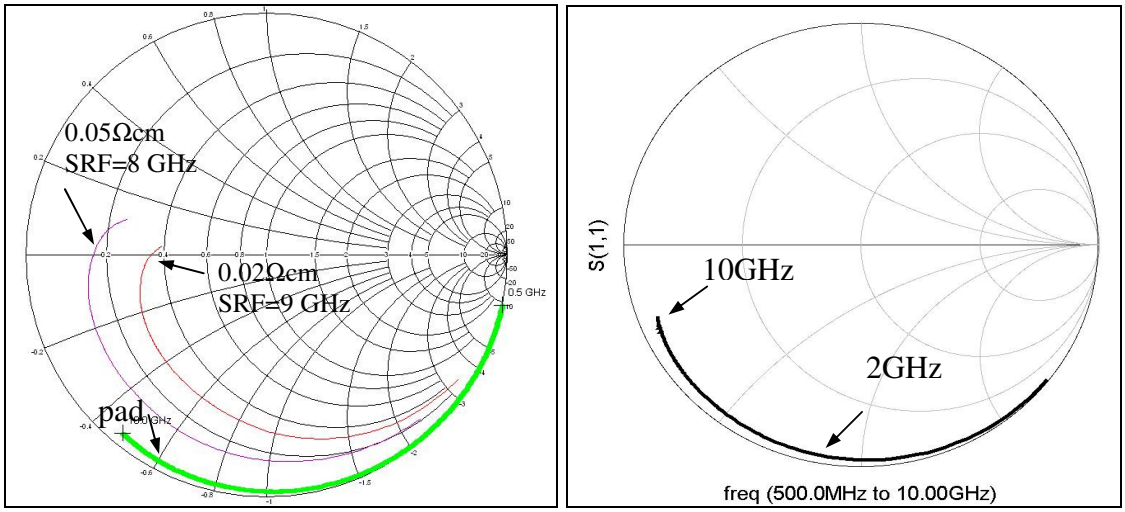
parameters for through calibration. It is important to minimize the return loss below -60 dBm (leakage-free cable, clean probe tips, and low contact resistance in the range of μΩ).



(a) (b)

Figure 3.16 a) Measured return loss, b) Measured insertion loss for the through calibration.

A Q of 49 is measured for a 60 μm thick capacitor at 1 GHz, which is close to the simulation. Figure 3.17 shows the measured return loss for the pad, and silicon varactor (left) and gold/Si varactor (right) in the frequency range of 0.5-10 GHz.

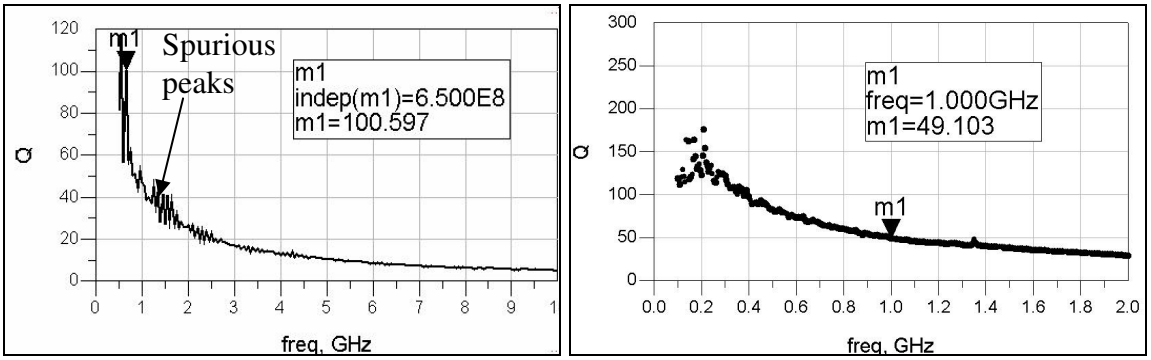


(a) (b)

Figure 3.17. Measured s_{11} of the HARPSS varactor, a) Before and b) After gold deposition.

The new probe tips that dig deep inside the metal instead of sliding over the metal give better loss since the extra loss associated with the metal surface roughness and

surface contamination will be eliminated. An IF bandwidth of 100 Hz with no averaging was used to minimize the spurious peaks. Figure 3.18 demonstrates the extracted Q in for two different HARPSS varactors. The return loss was measured to be below 0.5 dB at 1 GHz [96].



(a) (b)

Figure 3.18. Measured Q factor of two different HARPSS varactors [96].

The HFSS simulation for two different bulk conductivity is compared in Figure 3.19 to measurement for a HARPSS varactor. The silicon resistivity was 0.005 Ωcm. A close agreement between model and measurement exists especially at low frequencies.

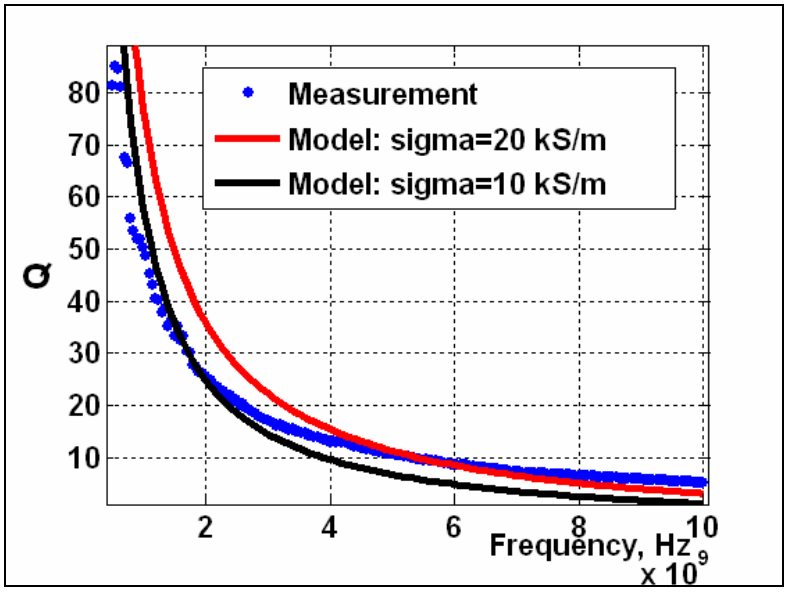


Figure 3.19. Measured Q vs. simulated Q for two different HARPSS varactors [97].

CHAPTER IV

MEMS PACKAGE DESIGN AND IMPLEMENTATION

The packaging technique that we present is a low cost encapsulation suitable for a variety of MEMS devices with reduced size electrical interconnections using polymer overcoats [99]. The method is applicable to both surface and bulk-micromachined structures, after their fabrication is completed. A cavity with scalable height is created on top of the movable/resonant part of MEMS by processing a sacrificial polymer, followed by overcoating the cavity by spin casting a low-κ polymer. The overcoat polymer is patterned to get access to the contact areas. The air cavity will be formed by thermolytic (multiple steps) degradation of the sacrificial polymer and permeating through the overcoat. For MEMS that need vacuum, a layer of gold is deposited and patterned over the polymer overcoat. The edges of the polymer overcoat can be tailored to have smooth transition to accommodate metal evaporation/sputtering/plating. Compared to the current overcoats used in MEMS and IC packaging, the polymer overcoat has superior properties, such as minimum dielectric constant and loss tangent, small moisture absorption, and high resistivity against chemical agents after curing. The overcoat geometry can be scaled to tailor different sizes of the MEMS up to a few millimeters in size. Using a low-loss overcoat makes the technology ideal for wide-band packaging of

RF MEMS passives and switches. The low temperature packaging technique is CMOS and biocompatible and it does not add any stress to the movable components, as well as the metal parts. The ability to pattern the overcoat, as opposed to bonding a capsule, provides the opportunity to shrink the interconnect dimensions to enable packaging of nanostructures.

The main advantages of our technique are:

(1) Low-temperature process, suitable for packaging of MEMS and CMOS devices that are sensitive to high temperature and thermally-induced residual stress.

(2) Low-cost polymer-based packaging that does not require wafer bonding, epitaxial growth or Low Pressure Chemical Vapor Deposition (LPCVD) of inorganic films, instead the method requires standard spinners, exposure tools, and ovens.

(3) Thermal decomposition of sacrificial material is used instead of wet etching, which is fast, reliable, structurally benign (no perforation), stiction-less, and CMOS compatible.

(4) The thickness of the sacrificial material and the polymer overcoat can be arbitrarily designed based on the device geometry, size and application.

4.1. Packaging Process Design

The packaging sequence is depicted in Figure 4.3 [99, 100]. Starting with released MEMS, as of Figure 4.1(a), the main packaging sequence consists of three main phases:

4.1.1. Cavity Formation using Unity Sacrificial Material

This phase is to form a cavity with desired height on top of active component of MEMS (e.g. electrodes, beams, tethers, proof mass, etc.), as shown in Figure 4.1(b).

Unity has good adhesion to most MEMS substrates, such as silicon, silicon dioxide, and metals. The cavity height can be in the order of 1-100 μm.

4.1.2. Polymer Overcoat Formation

The second main phase in the packaging sequence is to cover the cavity and the rest of the MEMS, with a compliant, negative-tone photodefinable polymer, as in Figure 4.1(c). A thin layer of PECVD SiO_2 is deposited on top of Unity patterns before polymer encapsulation to provide good mechanical strength of the cavity during decomposition. The bond pads are opened via patterning the polymer overcoat.

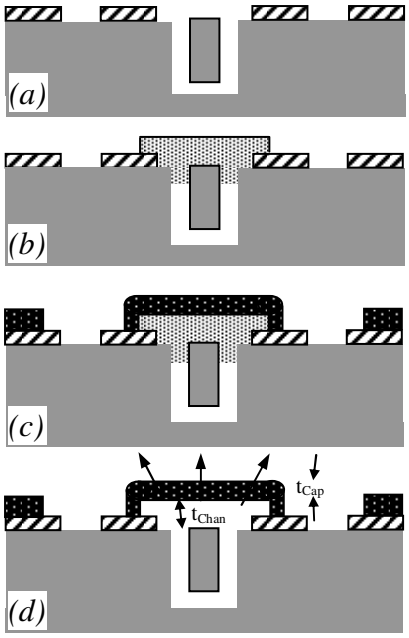


Figure 4.1. Polymer-based packaging sequence flow. (a): the released MEMS (b) after sacrificial polymer cavity formation, (c) after overcoat formation, (d) after decomposition [99].

It is possible to create thick (up to 500 μm) and pinhole-free encapsulation layer over large-area MEMS structures, which is very difficult to achieve by Chemical Vapor Deposition of films. The overcoat polymer can be selected among photodefinable polymers, e.g. Avatrel, benzocyclobutene (BCB), polymide, and SU-8. The mechanical

and electrical properties of the three mentioned polymers are compared in Table 4.1.

Table 4.1. Comparison between polymer overcoats.

	Avatrel	**Polyimide**	**BCB**
Moisture uptake, %	<0.1	0.5-3	0.23
Permitivity (ε_r)	4.50	3.1- 4.1	4.7
tan δ @ 1 GHz	0.009	0.01-0.015	0.015
CTE, ppm/°C	50	20	52
T_g, °C	>350	>430	>350

The most important properties for a packaging material are the following: high T_g, low loss tangent, low dielectric constant, low CTE, low stress (low modulus), low moisture uptake, and high thermal stability.

Avatrel 2195P is a photodefinable polynorbornene copolymer from Promerus LLC, consisting of a decylnorbornene and an epoxy norbornene [101]. The dielectric constant is measured to be between 2.5-3, and the loss tangent is about 0.009 at 1 GHz. It is observed that increasing the exposure dose will reduce the dielectric permittivity and loss. Higher dose will increase the crosslinking and so will reduce the dipole polarizations. Avatrel has a small moisture absorption, and can withstand temperatures as high as 260°C without considerable decomposition. Avatrel does not introduce significant thermal stress on the silicon substrate, after curing up to 180°C. Moreover, it has good adhesion to most of materials used in MEMS technology. The design of the overcoat shell plays an important role in the packaging. The flexibility in patterning the polymer overcoat, provides a wide range of overcoat geometries and heights with minimum interconnect size, a feature that is not possible by bonded capsules.

4.1.3 Decomposing the Unity Sacrificial Material

The last phase is to remove the sacrificial layer and form the embedded air cavity by thermal decomposition of the Unity sacrificial material at 200-260°C. This is the highest temperature step in the whole sequence. This step can be done in a regular oven with Nitrogen purging. The by-products of multiple-step decomposition are volatile gasses (e.g. O_2 and CO_2) that can permeate through the polymer at elevated temperatures (Figure 4.1(d)). A final metallization step can enable a hermetically sealed package. As depicted in Figure 4.1(a), this requires a hermetic insulator layer under the bond pads areas, to avoid the metal overcoat from touching the substrate. The best hermetic insulator is the silicon nitride deposited by LPCVD.

4.1.4. Sacrificial Polymer Processing

Processing the sacrificial material can be classified into four different approaches, used depending on the MEMS topology: These themes are known as packaging via patterning, dispensing, etching, or molding (see Figure 4.2 for details).

4.1.4.1. Packaging via Patterning (PVP)

The first method is more suitable for rigid and small MEMS devices such as SOI resonators that need a cavity wider than 20 μm. Figure 4.2(a) shows the packaging process sequence, referred to as packaging via patterning (PVP). The photo-definable sacrificial material, Unity 2000P [98] is first spin-coated and soft-baked. The Unity polymer is then patterned using Deep UV exposure (240 nm), followed by bake-developing at 110°C to decompose the exposed area.

4.1.4.2 Packaging via Dispensing (PVD)

The second sequence, referred to as packaging via dispensing (PVD), is described in Figure 4.2(b) and is used to package bulk micromachined structures with wide and deep cavities and/or fragile elements. Also MEMS devices with out of plane mechanisms need thick air cavities, which is possible with PVD. In this method, the sacrificial material (which does not have to be photo-definable) can be applied by a syringe-dispensing tool with adjustable droplet size (0.5 mm to 1 cm) to cover the cavity. Upon soft-baking, the Unity becomes solid and will support the released MEMS structure in the proceeding step. The PVD is especially suitable for large MEMS devices with delicate components that can break during spin coating of the sacrificial material; examples are HARPSS accelerometers and gyroscopes. Since the minimum dispensing nozzle size is about 0.5 mm, MEMS devices with size smaller than 0.5 mm can not be packaged with PVD. Moreover, MEMS that need access to center anchors (SOI ring and tuning fork gyroscope) can not be packaged using PVD, since dispensed droplet has to covers all the rings and electrodes. For the automatic dispensing tool, this limit is around 0.8mm.

Since Avatrel is transparent to visible light, this method can be used for packaging of large area optical MEMS devices, like micromirrors and optical switches

4.1.4.3 Packaging via Etching (PVE)

The third sequence, referred to as packaging via etching (PVE), is suitable for small area MEMS with wide/deep holes or fragile elements, e.g. HARPSS resonator, or RF tunable capacitors [96], and RF switches. In either case, in order to cover the wide

trenches or protect the fragile MEMS against breaking, spin coating the Unity at low speeds, or spin coating in multiple steps will be desired, which will tend to form thick Unity films. Patterning such a thick film to form fine cavities on top of beams has some limitations. It is difficult to form well-shaped thick Unity cavities with a width of less than 20 μm on top of trenches, so PVP will not be suitable. Instead, etching the Unity, using another mask is proposed. The mask can be a metal (e.g. titanium) or oxide deposited at low temperatures (e.g. 100°C) [98]. This mask should be etched in Buffered Oxide Etch, BOE (1:6 HF/H_2O), since BOE does not change the chemical properties of Unity and has no effect on clean decomposition.

As depicted in Figure 4.2.c, this method starts with spin casting the thick Unity, followed by deposition or evaporation of the hard mask, patterning the hard mask using SC1827, etching the mask in BOE, etching the Unity in oxygen plasma, and finally removing the hard mask in BOE. SC1827 will be removed during etching the Unity, so there is no need to strip it afterwards. Among several choices for dry etching the Unity, oxygen plasma works the best. Other gasses like CHF_3 tend to create some byproducts that may result in residues.

4.1.4.4 Packaging via Molding (PVM)

The last method is proper for nanostructures that need small and thin cavities. For these cases, none of aforementioned methods will work. As shown in Fig. 4.2.b, instead of spin casting the Unity, the packaging sequence starts with deposition of the oxide

mold, by PECVD, to overbridge the MEMS trenches. The oxide thickness defines maximum cavity height. This is followed by patterning the oxide with a negative resist with sharp sidewalls, and RIE etching the oxide. Then a thin layer of Unity can be spin coated and cured on top of the oxide. The thickness of Unity on top of cavity (t_{Cavity}) is larger than the thickness of Unity on top of mold (t_{Mold}), so oxygen plasma Reactive Ion Etching (RIE) with proper time can first remove the Unity on top of the mold and leave some Unity as the cavity. Finally the oxide mold is removed in BOE or by RIE, leaving a thin Unity with dimensions that can be in the sub-micrometer range. This method is proper for bulk micromachined MEMS with gap sizes in the order of 10 nm-1 μm.

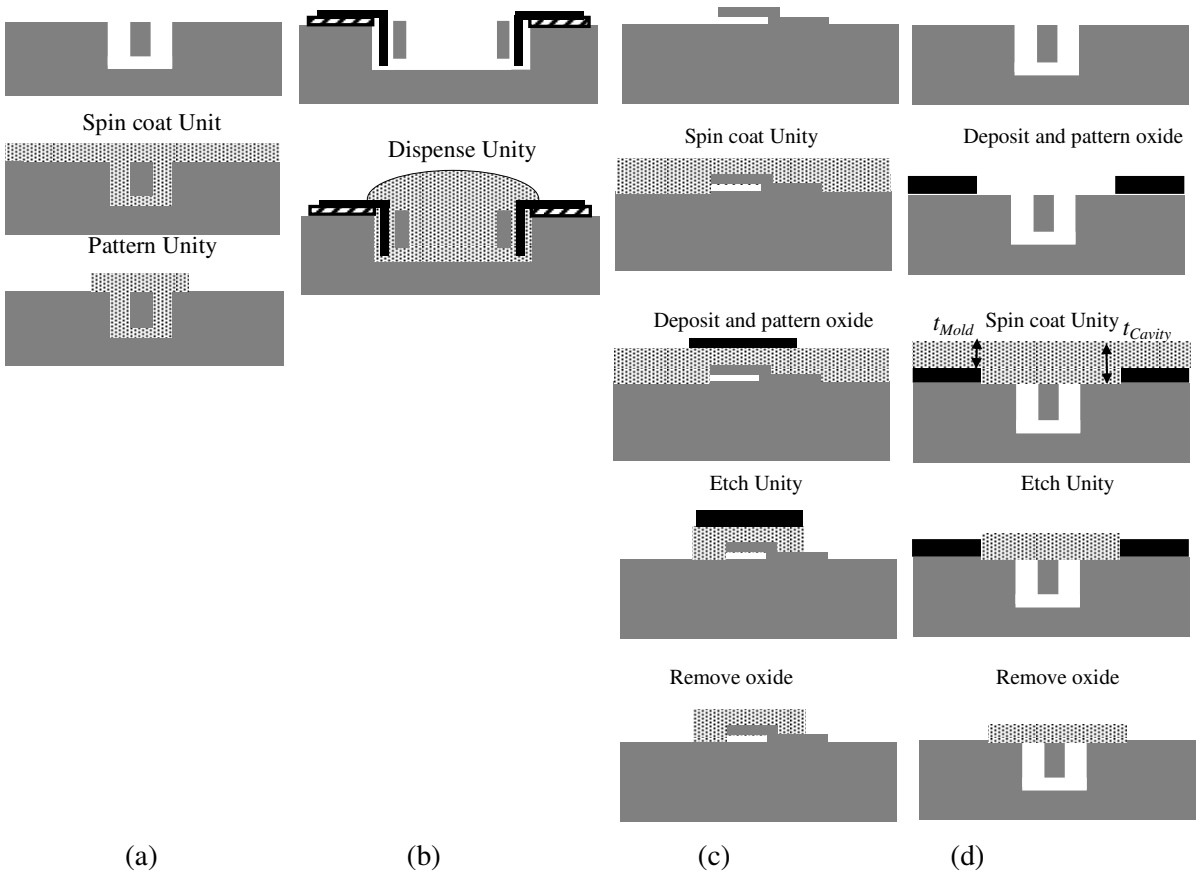


Figure 4.2. Process flow for sacrificial polymer processing: (a) PVP; (b) PVD; (c) PVE; (d) PVM [100].

4.2. Metal-Organic MEMS Package Design

In order for the overcoat to tolerate the pressure difference between inside and outside of the cavity, certain requirements should be considered when designing the overcoat geometry. Environmental conditions such as temperature change, thermal shock, molding pressure, or pressure difference between inside and outside cavity (Δp) will cause cap bending. A proper design for the metal-organic package shown in Figure 4.3 should guarantee that maximum cap bending (Z_{max}) is much smaller than cavity height (t_{Cavity}).

According to basic mechanics, the displacement (z) of a flat diaphragm with thickness h, under uniform pressure difference, can be modeled as in equation (4.1) [104]:

$$\frac{\partial^4 z}{\partial x^4}+\frac{\partial^4 z}{\partial y^4}+\frac{\partial^4 z}{\partial x^2 \partial y^2}=\frac{12\Delta p(1-\nu^2)}{Eh^3} \tag{4.1}$$

If the edges are fixed, then the maximum stress and z-axis displacement of a square plate can be stated in equation (4.2):

$$\sigma_{Max}=\beta(P_2-P_1)(\frac{W}{t})^2, z_{Max}=-\alpha\frac{(P_2-P_1)W^4}{Et^3} \tag{4.2}$$

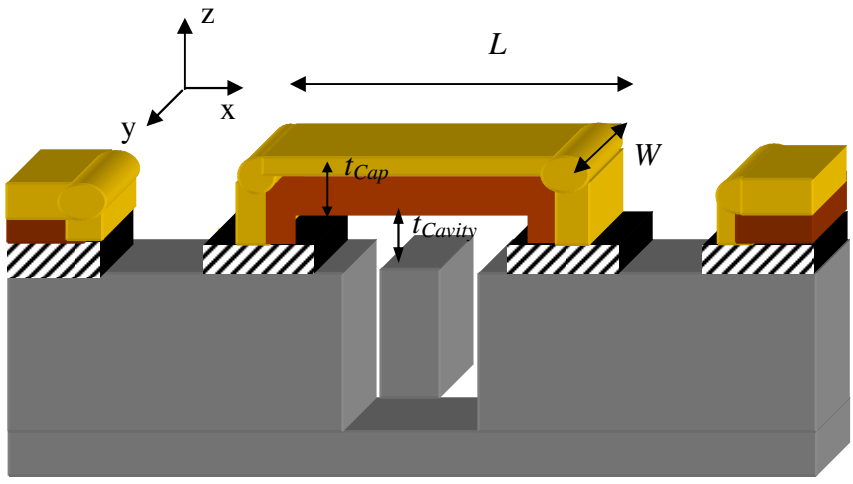


Figure 4.3. Geometry constraints, maximum out of plane stress, and maximum bending of the overcoat [103]

In equation (4.2), it is assumed that the deflection is much smaller than plate thickness and no residual stress or bending stiffness exists in the film. The coefficients α and β are dependent on plate aspect ratio and are 0.0138 and 0.3078 for a square plate, respectively. The above analysis considers bending due to flexural rigidity. For a more precise analysis, the effect of residual stress (σ) and in-plane stretching should be considered in determining the plate bending, as stated in equation (4.3) and (4.4) [105]. Equation (4.3) considers a square plate with length (L) and equation (4.4) is for a circular cap with radius (r). t_C is the film thickness, Z_{max} is the maximum bending, and E and ν are the modulus and Poission's ratio of the film.

$$\Delta p = \frac{3\pi^2\sigma_0}{2L^2} t_{Cap} Z_{\max} + \frac{2\pi^4 E}{3(1-\nu^2)L^4} t_{Cap}^3 Z_{\max} + \frac{\pi^4(7-2\nu)(5+4\nu)E}{128(1+\nu)(1-\nu)L^4} t_{Cap} Z_{\max}^{\ 3} \tag{4.3}$$

$$\Delta p = \frac{4\sigma_0}{r^2} t_{Cap} Z_{\max} + \frac{16\pi^4 E}{3(1-\nu^2)r^4} t_{Cap}^3 Z_{\max} + \frac{(7-\nu)E}{3(1-\nu)r^4} t_{Cap} Z_{\max}^{\ 3} \tag{4.4}$$

The three terms in (4.3) and (4.4) represent thin film residual stress, plate bending due to flexural rigidity, and in-plane stretching, respectively.

The packaging design includes the evaluation of the proper thickness of sacrificial polymer required to completely cover the MEMS without significant sagging, followed by calculating the minimum thickness of the overcoat required to tolerate the pressure difference, P. For the square overcoat caps with a cavity height, t_{Cavity}, the cap thickness, t_{Cap} should be designed so that the maximum plate bending (Z_{max} in equations (4.3) and (4.4)) is much smaller than t_{Cavity} [103]. This criteria is stated in equation (4.5):

$$t_{Cap} > \sqrt[3]{\frac{3(1-\nu^2)L^4}{2\pi^4 E t_{Cavity}} P} \tag{4.5}$$

Here E, ν, and L are the overcoat modulus, Poisson ratio, and length (For 10 μm thick Avatrel, E=1-2 GPa, and ν=*0.3*). The bending due to residual stress and stretching is neglected. In the resonator-packaging codesign, W=100 μm, L=220 μm, so α=0.0277, β=0.497, P≅1 atm=10^5 Pa.

The stress can be calculated using Stoney's equation (4.6) [106].

$$\sigma = \frac{1}{6}\frac{E_{Sub}}{R(1-\nu_{Sub})}\frac{t_{Sub}^2}{t_{Film}},$$

$$R = \frac{S^2 + 4X^2}{8X} \tag{4.6}$$

Here E_{Sub}, t_{Sub}, and ν are the Young's modulus, thickness, and poisons ratio of the substrate, respectively, R is the radius of curvature of the wafer measured by a contact profilometer, t_{film} is the Avatrel thickness (measured by a spectrometer), S is the stylus scanning range (5 mm), and X is the wafer warpage. In the trivial case, where t_{film}=0, X_{film} will be zero resulting in a zero stress. In order to study the thermal stress of the Avatrel overcoat, curing at 100°C, 200°C, and 300°C was performed and the Young's modulus was measured for each temperature using a Hysitron nanoindenter to be around 1.9 GPa for the cured Avatrel with a thickness of 10 μm. The result is shown in Figure 4.4.

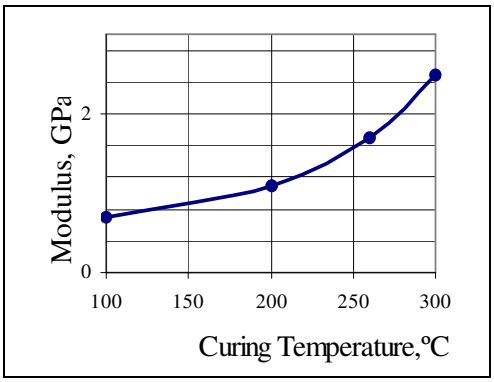


Figure 4.4. Measured Avatrel Young's modulus vs. curing temperature using nanoindenter

Thermal stress for 2-20 μm thick Avatrel that was cured at 200°C was obtained using Equation (4.6) in a KLA Tenkor contact profiler. The results are shown in Figure 4.5. A 10 μm thick Avatrel cured at 200°C has a residual stress of about 4.5 MPa.

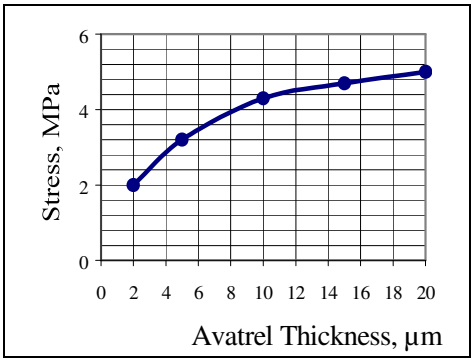


Figure 4.5. Avatrel stress characterization: calculated tensile stress vs. thickness of overcoat.

The electrical, mechanical, thermal, and optical parameters of Avatrel was measured and the summary of the measurements for 10 μm thick film are listed in Table 4.2. These include dielectric constant, modulus, Poisson's ratio, volume density, glass transition temperature, and index of refraction. The small dielectric constant of Avatrel is suitable for low-loss RF MEMS packaging. The glass transition temperature of Avatrel (~300°C) is much higher than that of Unity (~100°C).

Table 4.2. Measured physical parameters for Avatrel [103]

		Equipment
Electrical		
Permitivity at 1GHz	2.57	hp network analyzer
Mechanical		
Young's modulus (at 25°C)	1.9GPa	Hysitron nanoindenter
Poisson's ratio	0.3	Hysitron nanoindenter
Volume density	1.52g/cm^3	Milligram meter
Thermal		
Glass transition temperature	300°C	KLA Tencor profilometer
Optical		
Index of refraction	1.5-1.6	Woollam ellipsometer

The next step is modeling the beam bending in an Avatrel cap due to an atmosphere pressure difference. All edges of the diaphragm are fixed. As shown in Figure 4.6, even for a large structure like a gyroscope with 3 mm diameter, the maximum bending for a 100 µm thick Avatrel is still less than 60 µm. Using L=3 mm, t_{Cavity}=30 µm E=2 GPa, ν=0.3, P=10^5 Pa in equation (4.5) yields: t_{Cap}>100 µm.

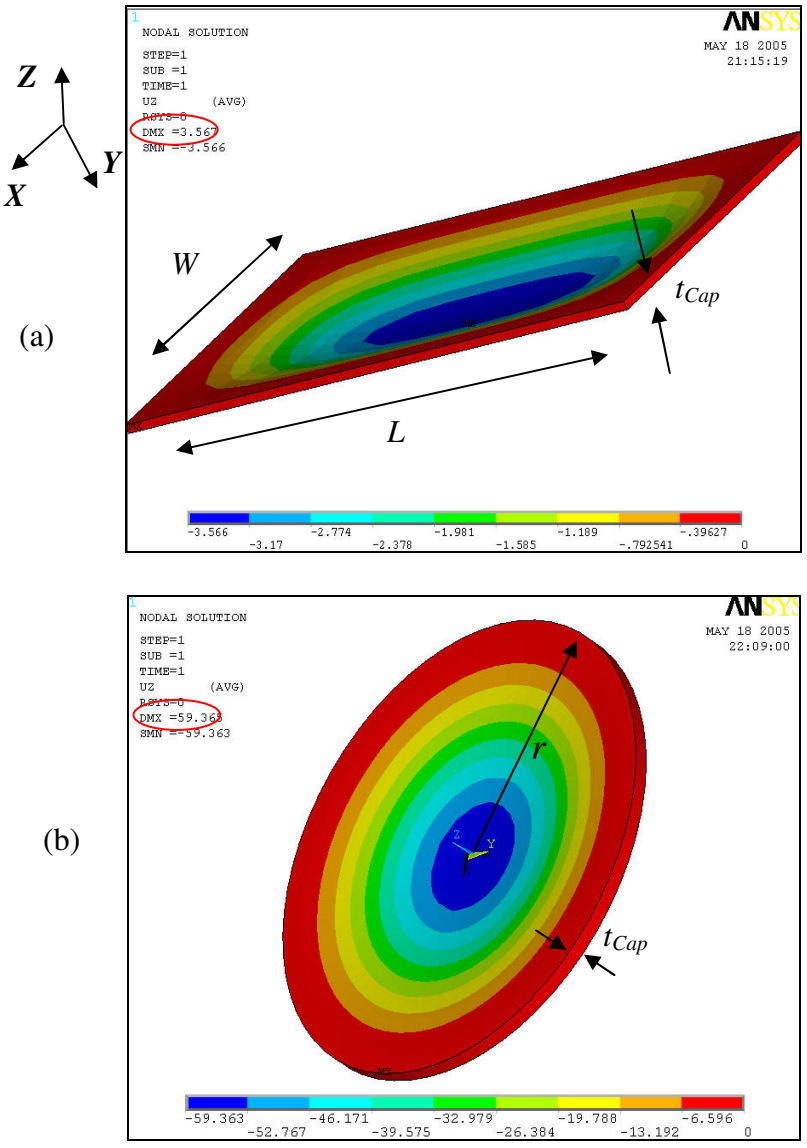


Figure 4.6. Deformation of the Avatrel cap with fixed edges under 1 atm pressure difference: a) Rectangular cap with t_{Cap}=10 µm, L=250 µm, W=100 µm; b) Circular cap with t_{Cap}=100 µm, r=1.50 mm [100].

An alternative method for near-hermetic packaging without etching the metal overocoat is shown in figure 4.7. After decomposing, a metal film that is thinner than Avatrel is directly evaporated. Because of the 90° profile of the Avatrel overcoat, the metal on top of the package will be isolated from the metal evaporated elsewhere. This method eliminates the step needed to pattern metal. The air or water molecules can penetrate through the Avatrel sidewalls that are not covered with metal at elevated temperatures. This method is suitable for MEMS that do not need vacuum packaging such as varactors or accelerometers.

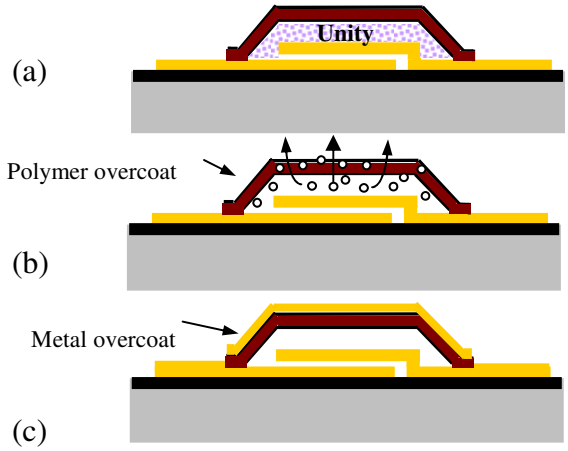


Figure 4.7. Alternative method for hermetic packaging, a) Unity and Avatrel patterning, b) Unity decomposition, c) Metal evaporation [103].

4.3. Packaging of Microresonators

After silicon bulk micromachining techniques were introduced, SCS has become an attractive material for MEM resonant devices due to the advantages such as high intrinsic *Q*-factors and long-term stability. Different types of SCS resonators with sub-micrometer gaps can be made through the HARPSS process in silicon substrate [77]. Flexural beam resonators can be also made on low resistivity Silicon-on-Insulator (SOI) substrates.

For a clamped-clamped beam resonator operating in vacuum, with width w, thickness t, and length l, the first resonance mode, ω_1, is described in (4.7) [91]:

$$\omega_1 = 22.37\sqrt{\frac{E}{12\rho}}\frac{w}{l^2} \tag{4.7}$$

Figure 4.8 shows the equivalent RLC circuit of a beam resonator with equal sense/drive gap sizes. All the elements (e.g. motional resistance) vary with body voltage.

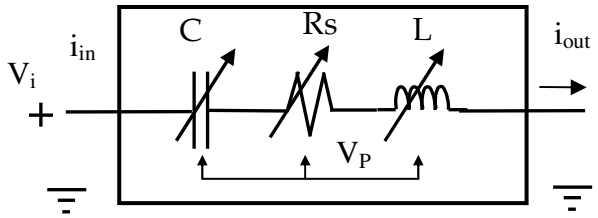


Figure 4.8. Resonator simplified equivalent circuit for equal sense/drive gap spacing.

The transfer function of the circuit in the frequency domain is as the following:

$$Y_{oi}(s) = \frac{i_{out}}{V_i}(s) = \frac{\frac{s}{L}}{s^2 + 2\xi\omega_1 s + \omega_1^2} = \frac{\frac{s}{L}}{s^2 + \frac{R}{L}s + \frac{1}{LC}} \tag{4.8}$$

Here ξ is the damping factor associated with support loss and thermoelastic damping.

The measured unloaded mechanical Q_U, and the squeeze film damping coefficient, D, can be formulated in (4.9) terms of electrical and mechanical parameters of the resonator:

$$Q_U = \frac{E_{Total}}{E_{Lost}} = \frac{1}{R}\sqrt{\frac{L}{C}}, \qquad D = \frac{2}{\xi} = \frac{\omega_1 M}{Q_U} \tag{4.9}$$

The RLC parameters can be extracted from the measured Q, beam width/length/thickness, $W/l/t$, beam stiffness, K, drive gap, g, drive (sense) capacitance, C_d (C_s), polarization voltage, V_p, and electromechanical coupling coefficient, γ [91].

$$R = \frac{Dg^2}{C^2_{d,0}V_P^2} = \gamma\frac{\sqrt{KM}\,g^4}{Q(\varepsilon_0 ltV_P)^2}, C = \frac{C_d^2 V_P^2}{Kg^2 - V_P^2(C_S^2 + C_d^2)}, L = K\left(\frac{g}{V_P C_d W}\right)^2 \tag{4.10}$$

The RLC parameters for three different types of beam resonators are listed in Table 4.3. Q_{Supp} represents the support or clamping loss, during vibration, shear forces and

moments are exerted on clamp ends, and will excite elastic waves to propagate into the supports and create support loss. Other mechanisms limiting the overall Q are thermoelastic dissipation due to irreversible heat flow across the beam thickness, and surface loss due to the disruption of the atomic lattice at surface or a thin layer of contamination.

Table 4.3. Extracted circuit parameters for the SOI beam resonators.

Type	f_0, MHz	R, MΩ	L, H	C, aF	Q_{Supp}	Q_{Meas}(avg)
W=7 μm, L=208 μm	1.381	13.096	6031	2.2	16738	6000
W=7 μm, L=150 μm	2.656	18.16	4350	0.825	6277	5500
W=7 μm, L=94 μm	6.7621	28.98	2728	0.2	5998	5000

4.3.1. Resonator Packaging Results

The sub-micron high aspect-ratio gaps are created by Deep Reactive Ion Etching (DRIE) of silicon in an Inductively Coupled Plasma (ICP). Figure 4.9 shows SEM view of a SCS clamped-clamped beam resonator. As explained in section 4.1, the LPCVD nitride has been used as a hermetic insulator, and has been removed on top of bond pads and the resonant beam.

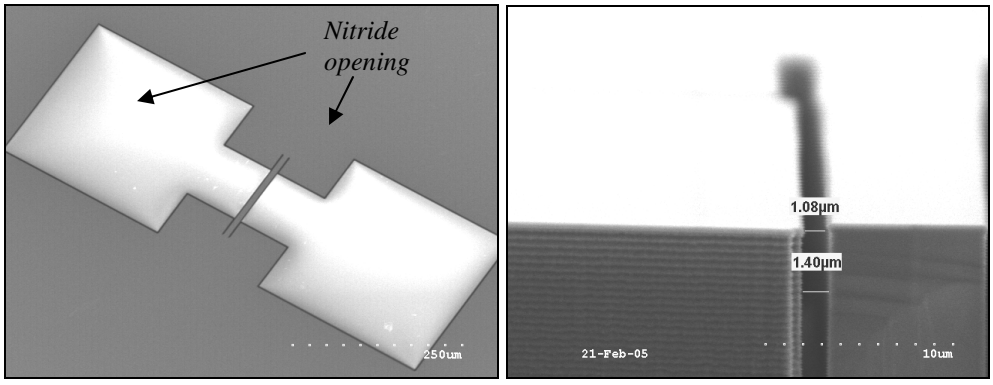


Figure 4.9. SEM view of: a) 200 μm long, 8 μm wide, 25 μm thick SOI beam resonator with 1 μm gap size and 0.1 μm thick nitride film, b) The 1 μm capacitive gap defined by DRIE.

HARPSS technology can create higher aspect ratios, exploiting the thickness of a sacrificial oxide layer. These resonators have wide etch-pits to release the devices. Packaging of such devices requires applying a thick Unity.

Figure 4.10 shows the pre-packaging testing of a 2.5MHz resonator inside a vacuum probe station at the wafer-level. The *Q* factor has been recorded using an HP5017 network analyzer in a tow port (three probe tips) configuration by applying a polarization voltage of 20-70 V for the 3 MHz resonator and 40-120 V for the 7 MHz resonator to the device layer. The beam can be polarized directly or indirectly by capacitive coupling. This frequency (7-10 MHz) is believed to be the higher limit (highest tolerable motional resistance) for the flexural beam resonators made by DRIE. To get to higher frequency ranges, other resonator types including block, ring, disk, or FBAR should be used.

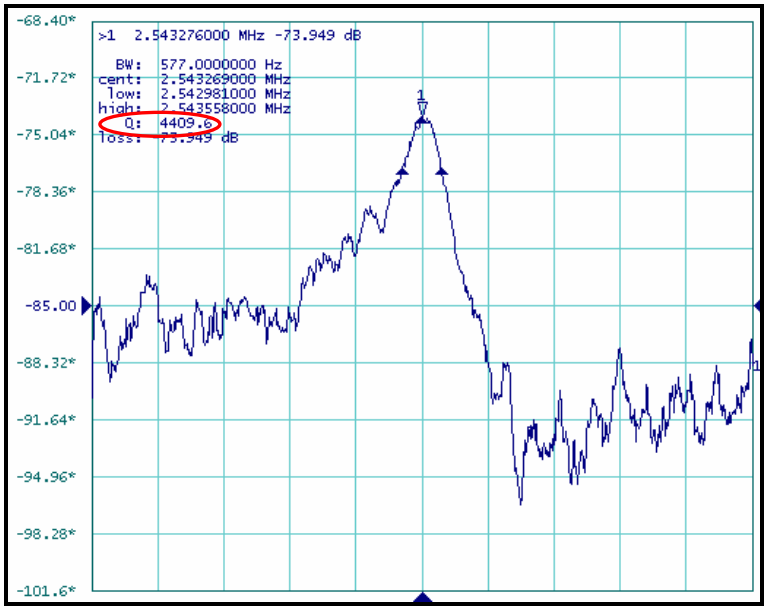


Figure 4.10. RF responsivity of a 2.5 MHz resonator (with island: the beam is isolated from the substrate). Test setup parameters are: signal=10 mV_{p-p}, IF bandwidth=10Hz, and Vp=90V.

The *Q* factor is limited by Q_{supp} and Q_{TED}, but if it operates in atmosphere, the viscous damping will be the dominating loss mechanism. As Figure 4.11 shows for several

different beam resonator designs, a vacuum level of at least 5 Torr is required for oscillations to start with a measurable Q (>1000). The tunability of the 3 MHz resonators is about -91 ppm/V and the temperature dependency is around -30 ppm/°C.

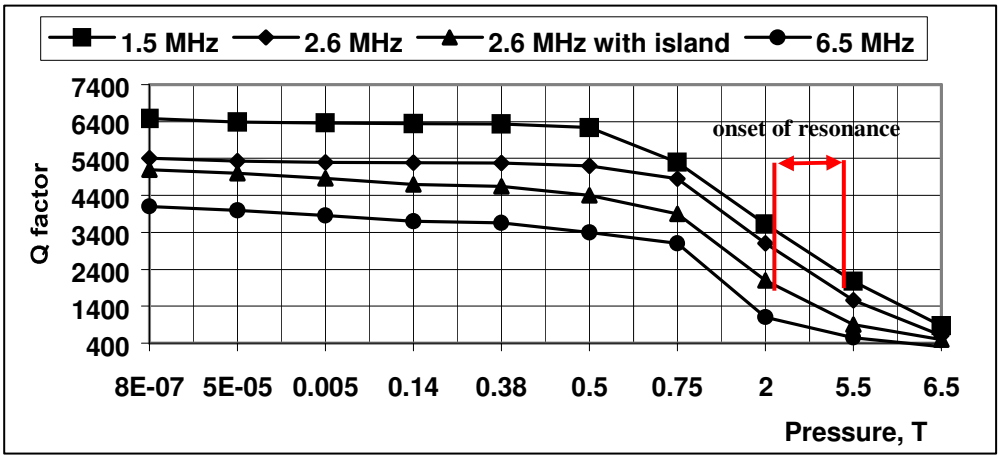
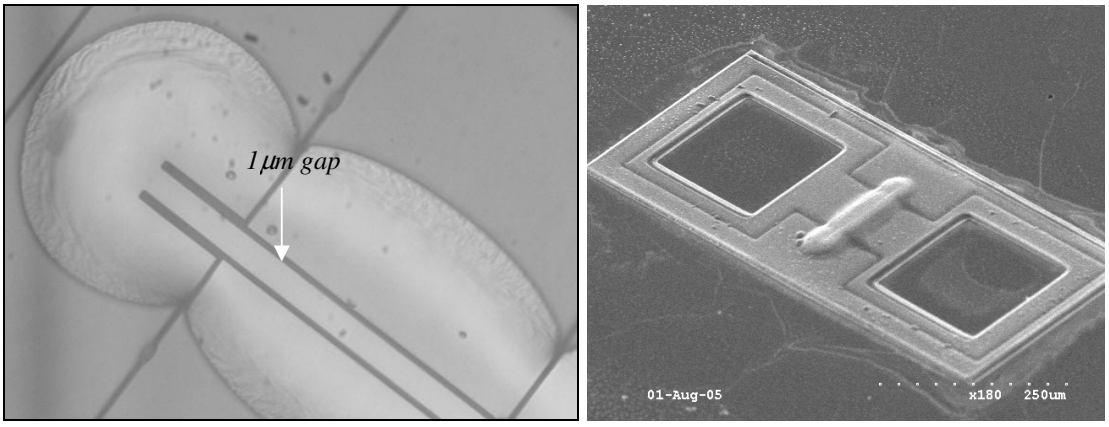


Figure 4.11. Average Q factor versus pressure for different SOI resonators before packaging, recorded before packaging.

The plots in Figure 4.11 have been collected by direct probing in a vacuum probe station equipped with a heater, therefore the Q is slightly lower than wire bonded Q due to lower SNR in such a system. The dotted line shows the range of Q that can be measured in the network analyzer. The test setup is shown in Figure 4.12. The probe station is equipped with a heater to heat the resonators while evacuating the package.

Figure 4.12. Test setup for characterization of resonators in vacuum.

To demonstrate the PVP technique, shallow SCS beam resonators were fabricated and encapsulated. Figure 4.13 shows the close-up view of a 15 μm thick, 8 μm wide, 150 μm long beam resonator with 1 μm gap spacing after decomposing Unity and after PVP packaging using aluminum/Avatrel package.



(a) (b)

Figure 4.13. a) View of the clean cavity after decomposition of Unity, b) View after packaging using 4 μm thick aluminum and 10 μm thick Avatrel on a 10 μm tall cavity.

The air cavity has been covered with 10 μm thick Avatrel to optimize the decomposition step and evaluate the polymer processing method. To perform a successful vacuum packaging for the same type of beam resonators, two extra conditions have to be met: an extra LPCVD nitride should be used as insulator, and all the isolation trenches must be covered with Avatrel, as shown in Figure 4.14.

Figure 4.14.a is the resonator before packaging, Figure 4.14.b is the same resonator after covering the beam with Unity, Figure 4.14.c shows the vacuum packaged resonator, and finally Figure 4.14.d is the cross section of the 25 μm thick SCS beam, the 15 μm tall embedded vacuum cavity, the 12 μm thick polymer and the 1 μm titanium/gold cap.

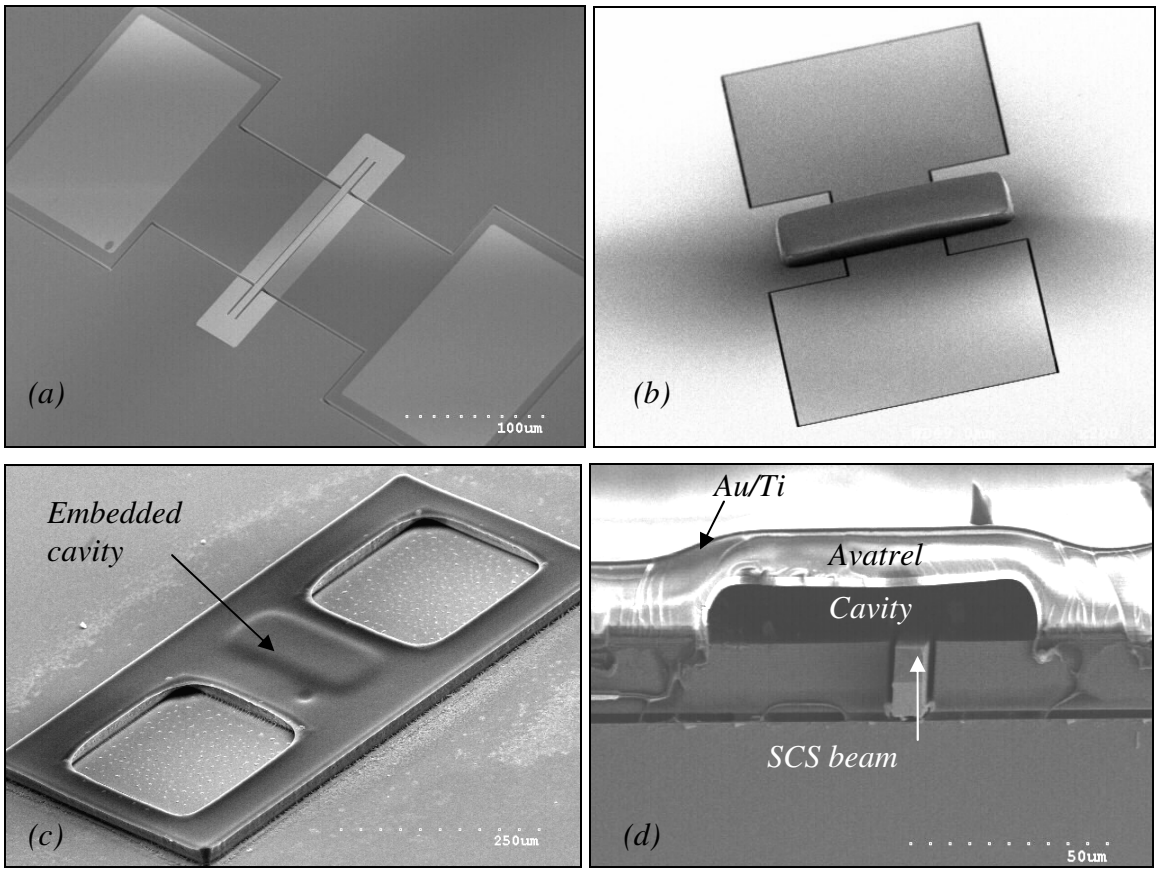
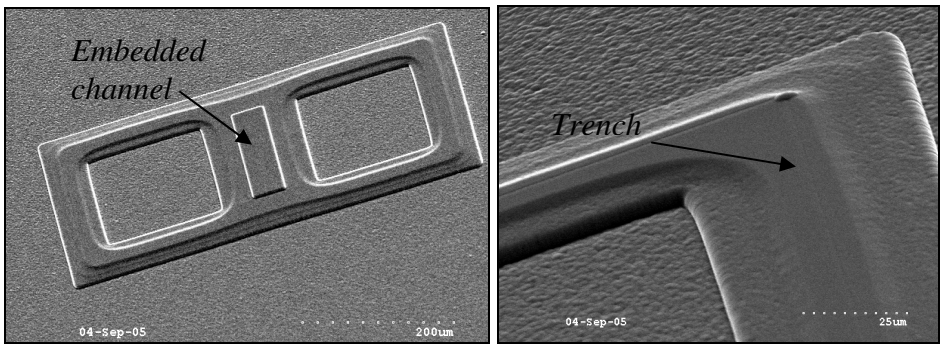


Figure 4.14. Vacuum packaged resonator: a) Before packaging, b) After Unity patterning, c) After packaging, d) Cross section of the cavity and 12 µm/1 µm metal-organic bridge [100].

The Avatrel polymer was photo-exposed using i-line (365 nm) lithography and developed in a spray developer, followed by a short descum in oxygen plasma. The structural cracks in the cap after metal deposition happen because of outgasing of solvents during plasma deposition. Also the difference in CTE of Avatrel (40-50 ppm/°C) and silicon (3 ppm/°C) can cause warpage in Avatrel. The warpage can be reduced by using a very gentle cooling down after decomposition. The cracks can be reduced by in-situ heating of Avatrel during metal deposition and reducing the plasma power. Figure 4.15 shows a resonator packaged through PVM. The package consists of 1 µm/10 µm chromium/Avatrel and is free of cracks. CTE of chromium is close to CTE of silicon.



(a) (b)

Figure 4.15. (a) Packaged resonator using PVM (10 μm/1 μm chromium/Avatrel), b) Perfect coverage of trenches with Avatrel, no footing, or metal cracking can be observed.

The resonators were arranged in a configuration shown in Figure 4.16 to be compatible with leadframe assembly. The resonators will undergo plastic molding process. Photodefining the polymer cap, as opposed to bonding the cap, provides small horizontal feedthroughs (no bond rings) and a rigid package to survive the plastic molding pressure (70-80 atm) and temperature (175-180°C) [102].

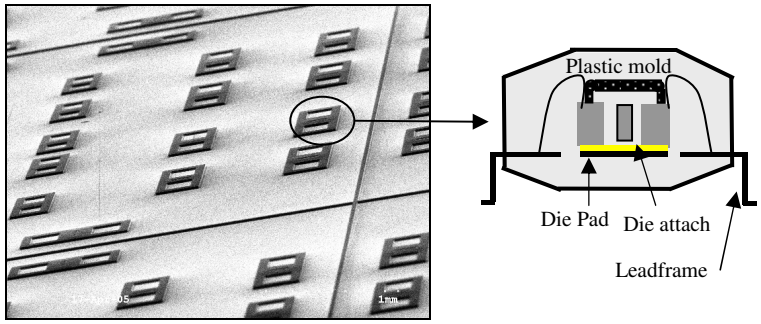
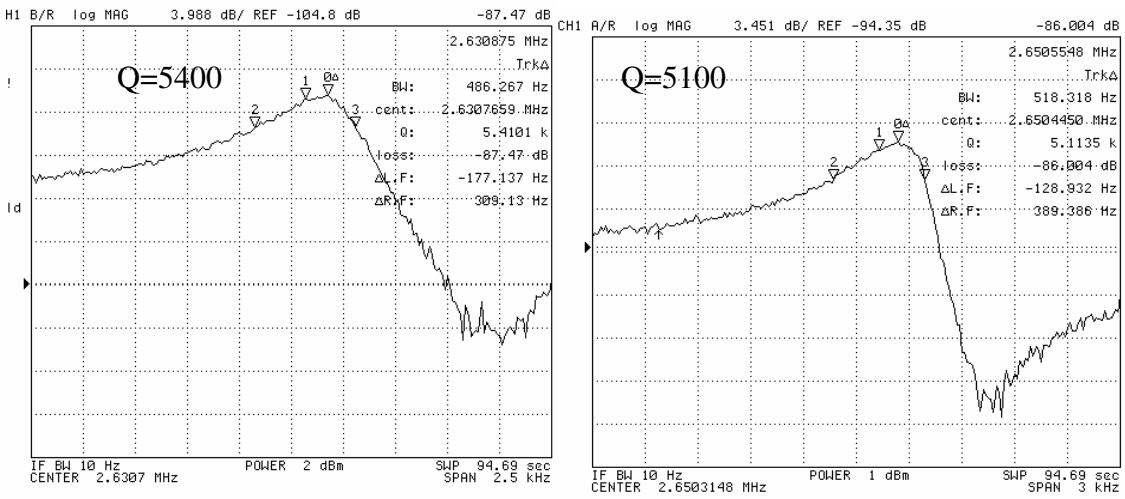


Figure 4.16. Packaged resonators in a die compatible with leadframe assembly [100].

The resonators were tested in the wafer-level before and after packaging. Figure 4.17.a and b show the frequency response of the resonator in vacuum before and after packaging. The *Q* factor and the resonance frequency (2.6 MHz) did not change significantly, proving that decomposition does not leave any residues inside the gap.



(a) (b)

Figure 4.17. Frequency response of a 15 μm thick resonator; (a) Before and, (b) After PVP [99].

Table 4.4 gives a summary of twelve resonators tested before and after packaging in the middle die. In the table, f_u (f_p) is the resonance frequency before (after) packaging and Q_u (Q_p) is the quality factor before (after) packaging. . In average, the fundamental resonant frequencies of the tested microresonators decreased about 1.3% after packaging. Some degradation in Q factor after encapsulation is believed to be due to small residues of the sacrificial polymer on the beam surface, which can increase the surface loss (since the polymer is of different type than the resonator).

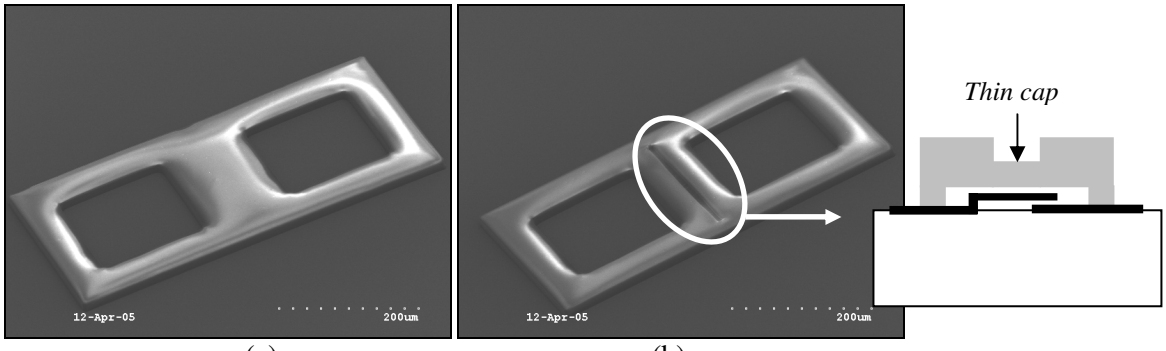
Table 4.4. Test results of ten package resonators in the middle of a 4" wafer [101]

Resonator	**Testing before Packaging**		**Testing after Packaging**		**% degradation in Q**
	f_u *(MHz)*	Q_u	f_p*(MHz)*	Q_p	
1	2.513379	5800	2.517405	4045	30.26
2	2.543391	4552	2.543269	4409	3.14
3	2.526077	4566	2.522788	3192	30.09
4	2.548593	4717	2.517405	4045	14.25
5	2.561697	2948	2.556300	2716	7.87
6	2.561697	1194	2.565870	920	22.95
7	2.558827	4522	2.556300	2716	39.94
8	2.57342	5150	2.573376	3807	26.08
9	2.55774	4922	2.55785	3772	24.38
10	2.56234	4012	2.56222	3742	6.73

However, this phenomena is difficult to be quantified. This can be confirmed by depositing of a thin layer of LPCVD nitride on top of an unpackaged beam, which results in Q reduction. The packaging yield (fraction of the packaged beams which resonated) was greater than 80% in our laboratory environment, The reduction in yield after packaging may be due to the non-ideal shape of the air-cavity in some resonators because of the misalignment or lithography errors, and not due to the packaging process [101].

The next step in characterization of the capped resonators was to determine how long it takes to create the required level of vacuum inside the embedded cavity to start resonance with high-Q. This has been done for three batches of resonators. The two factors that have significant effect on the evacuation time are the overcoat thickness and the temperature. As expected, heating up the substrate using a vacuum station equipped with heater, can reduce the time to start oscillations. Increasing the temperature will increase pressure difference and gas diffusivity, which will accelerate the evacuation.

In order to characterize the Avatrel permeability, different resonators have been packaged on the same die, having different Avatrel thicknesses, as shown in Figure 4.18.



(a) (b)

Figure 4.18. View of the packaged resonators used for intermediate testing, (a) View of the simple overcoat (15 μm thick), (b) View of the overcoat with thin (5-7 μm thick) cavity coverage.

Figure 4.18.a shows a capped resonator with the complete coverage of trenches with uniform overcoat thickness. The released Avatrel cap in Figure 4.18.b has a thinner

Avatrel (about 5-7 µm). A thin Avatrel cap provides shorter decomposition time and shorter outgassing time. As shown in Figure 4.19, for the 20 µm thick Avatrel, it takes two hours at room temperature and 1.5 hours at 150°C to start the oscillations. RIE was used to thin the Avatrel and form different thicknesses.

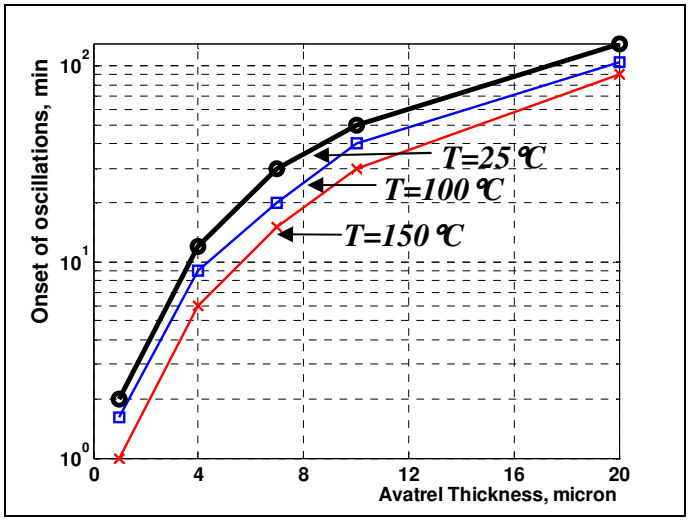


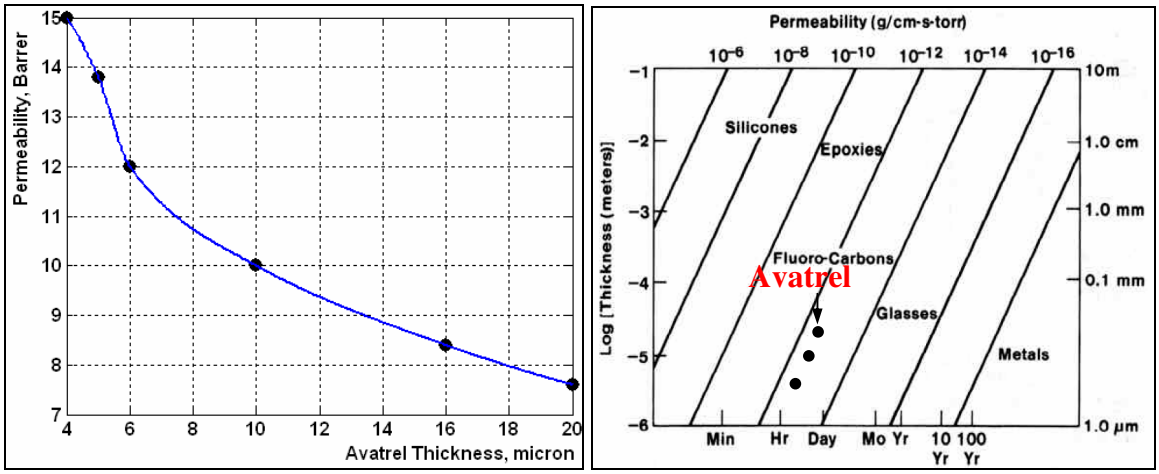
Figure 4.19. Evacuation time vs. Avatrel thickness for different substrate temperatures [100].

Gas permeation rate, P_G, of a membrane with thickness, t_{Cap}, and area, A_{Cap}, placed between two media with pressure difference of Δp and gas flow of F, can be defined as in equation (4.11) [100]:

$$P_G = \frac{F t_{Cap}}{A_{Cap} \Delta p} \tag{4.11}$$

Δp and F are assumed to be functions of time with the same form (e.g. inversely proportional to time) so that P_G is time independent. The evacuation time, t_s, is the time needed to create a vacuum level of better than 3-5 Torr to start the oscillations (Figure 4.11). From Figure 4.19, a value of t_s=3000 s is obtained for t_{Cap}=10 µm. Applying the values for F, t_{Cap}, A_{Cap}=0.02 mm^2 *and* Δp=3 Torr in (4.9) results in an average nitrogen

permeability of P_G=1.29×10^{-13} g/cm.Torr.s, (10 Barrer) for the 10 µm thick Avatrel [100]. Same procedure is performed to obtain gas permeability for different thicknesses, as shown in figure 4.20.a. There is an uncertainty in the calculation of average permeability due to acceptable range of 1 to 5 Torr for Δp in (4.9). A different method reported a nitrogen permeability of 4.3 Barrer for 100 µm thick polynorbornene (same polymer structure as Avatrel) [107]. As shown in figure 4.20.b for known materials, Avatrel curve lies within Fluorocarbons.



(a) (b)

Figure 4.20. a) Measured nitrogen permeability of Avatrel for different thicknesses, b) Permeation rate of known materials along with experimental data for Avatrel [100].

Depositing metal overcoats is one of best techniques to add hermeticity to the surface-micromachined MEMS package [29]. Presence of microcracks in the metal overcoat can cause vacuum leakage, which can be avoided by using a metal film with low residual stress and close CTE to the substrate, such as chromium. As listed in Table 4.5, chromium has the closest CTE to silicon (*CTE* (Si)=2.8 ppm/°C), largest modulus (*E*) and largest resistivity (ρ), and has good environmental resistance, but is a ductile metal. Gold, titanium, and platinum are the most resistive to environment. Alloy 42 is a nickel iron alloy for standard electronic packaging. Gold/titanium, copper/chromium, aluminum, and

chromium caps were tried as metal overcoats. To avoid microcracks in the polymer overcoat, metal deposition variables were optimized (power=100 W, and pressure= 7 mTorr). No significant cracks can be observed in the chromium-Avatrel cap after thermal cycling (5-10 cycles, 1 hour dwell time) from room temperature up to 200°C.

Table 4.5. Comparison of different metal overcoats [100].

Metal	Cr	Au	Al	Cu	Ti	Pt	Alloy 42
CTE, ppm/°C	4.9	14.2	23.1	16.5	8.6	8.8	6.0
E, GPa	279	79	70	140	110	168	144
ρ, μΩcm	12.5	2.2	2.65	1.68	4.2	10.5	70
ν	0.21	0.44	0.35	0.34	0.32	0.38	0.25

Figure 4.21 shows the residual stress measurement after annealing for sputtered aluminum, gold, and chromium on silicon substrate, measured by a contact profiler. The bending of the wafer prior to metal deposition is measured and subtracted from the post-deposition wafer to measure the film stress. The profiler uses substrate modulus, and film thickness to automatically measure the stress.

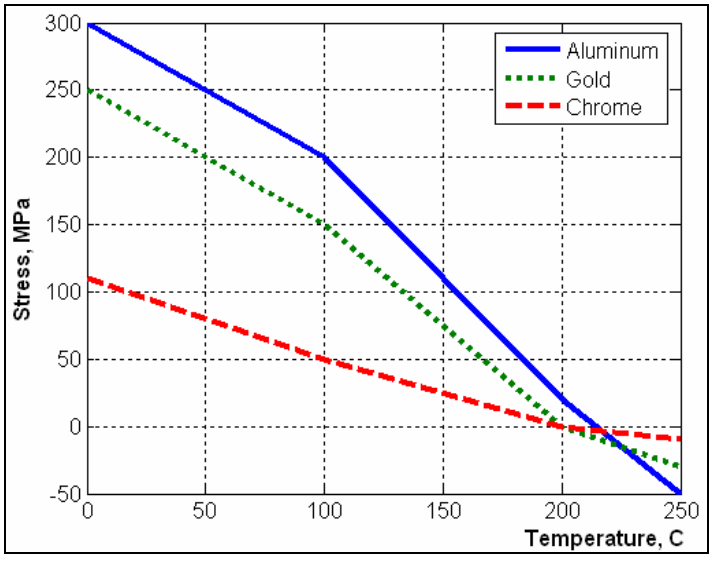


Figure 4.21. Stress characterization of 2.5 μm thick sputtered metal films on silicon using a KLA Tenkor contact profiler [100].

Curing the metal-organic package can be performed during metal deposition or after metal etching. The non-cured chromium cap shows a residual stress of 100 MPa. The thin-film stress of the metal film deposited at room temperature is always higher than the electroplated film [29]. The tensile stress drops to zero at 200°C and becomes compressive above 210°C. This stress reduces the total bending (Z_{max}). Z_{max} for the chromium-Avatrel cap in the device center was measured using a Wyko optical profiler for different metal thicknesses in a number of vacuum packaged resonators (Figure 4.22). The decomposition was done at 250°C, the polymer package was pre-cured at 180°C inside the deposition chamber to smooth out the sharp edges, the chromium deposition was started after waiting for about an hour at a pressure of around 6 mTorr and power of 80 W.

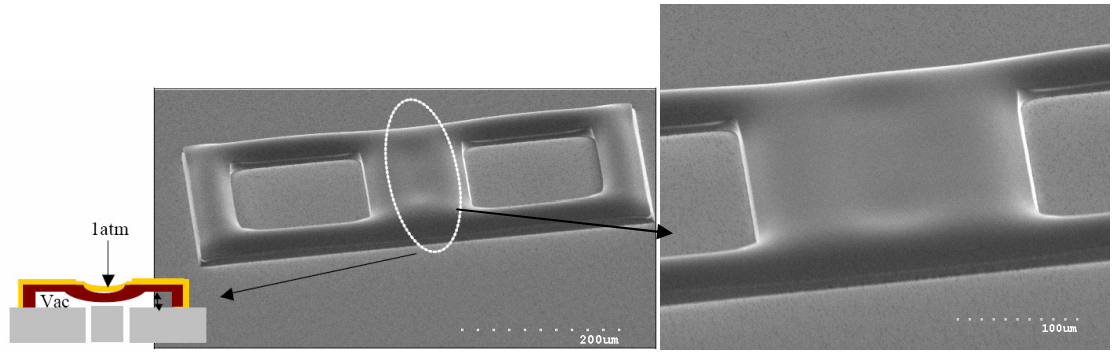


Figure 4.22. View of chromium-Avatrel cap bending under 1 atm pressure for $t_{Chromium}$=2 µm, $t_{Avatrel}$=8 µm, t_{Cavity}=7 µm [100].

As demonstrated in the Figure 4.23 for a packaged resonator with a 0.00015 mm^3 cavity, a sub-micron metal-organic cap can bend down as large as few microns in atmosphere, as a result of pressure difference. The measurements were obtained using a Veeco optical profilometer. For vacuum levels above 1 Torr, Z_{max} can be used to roughly estimate the cavity pressure level [100].

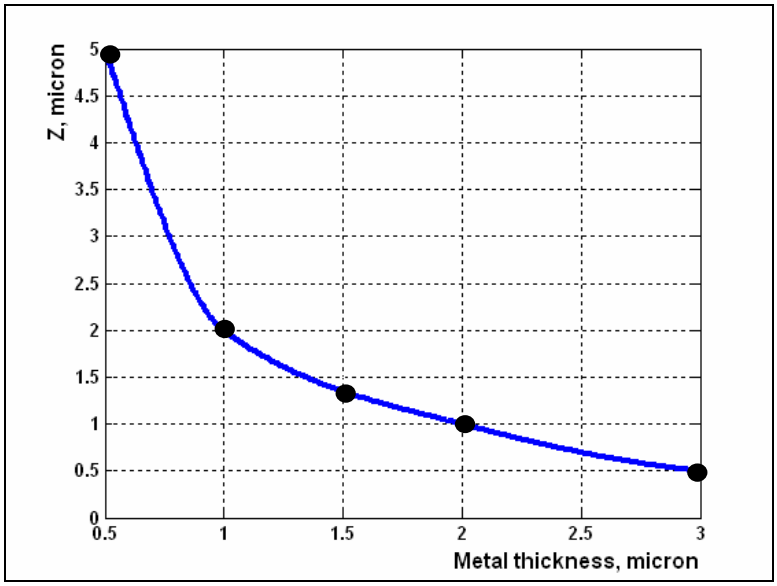


Figure 4.23. Optical measurement of Z_{max} for chromium-Avatrel cap versus chromium thickness using a Wyko optical profiler after vacuum packaging [100].

As shown in Figure 4.24, for the 0.5 µm thick chromium package, a pressure difference of 0.93 atmosphere results in Z_{max}=5 µm. Therefore the cavity pressure is estimated to be about 50 Torr (0.07 atm.).

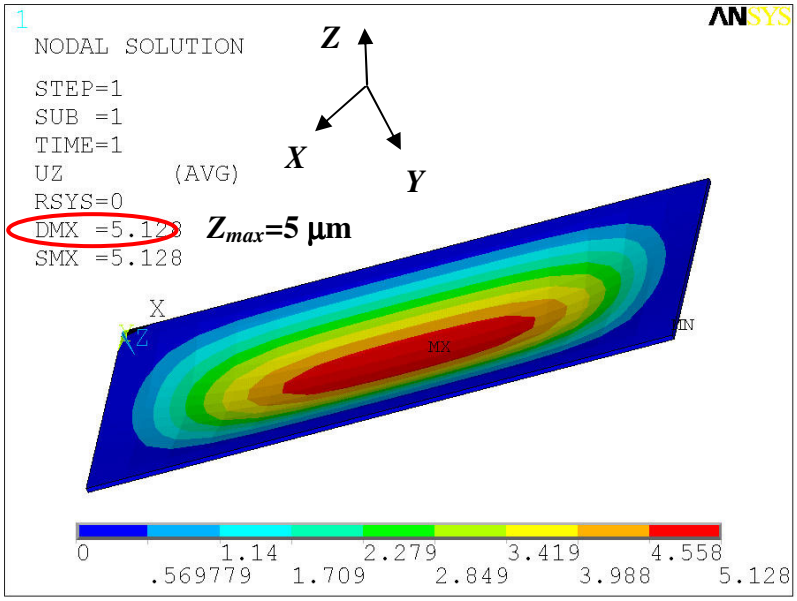
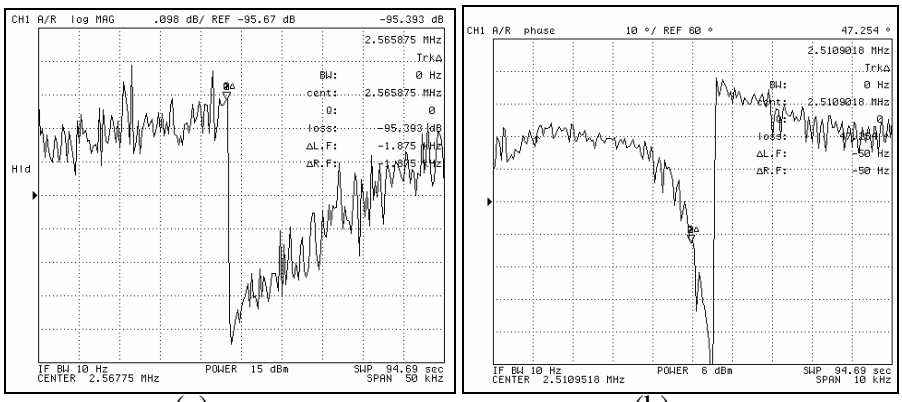


Figure 4.24. FEM simulation of deflection of the 0.5 µm thick Chromium package under a pressure difference of Δp=0.9 atm ($p_{outside}$=760 Torr, p_{Cavity}≅50 Torr) [100].

4.3.2. Residue Analysis for the Packaged Resonators

Decomposing at temperatures lower than 150°C resulted in non-working resonators. Figure 4.25 shows the frequency response of one of these resonators. Figure 4.25.a is the magnitude response; even 15 dBm drive and 80 V polarization voltage was not enough to pull up the amplitude into the detectable range. However, Figure 4.25.b shows that the resonance is the actual mechanical resonance. For the first resonance mode, the resonance happens sooner than the anti-resonance, and the phase shift is negative.



(a) (b)

Figure 4.25. Frequency response of the non-working packaged resonator: a) Amplitude response, b) Phase response.

The reduction in Q is believed to be caused of small residues left on the beam surface that can increase the surface loss. As shown in Figure 4.26, Q after packaging (Q_P) is always lower than unpackaged Q (Q_U). Therefore, the vibration amplitude of the packaged resonator ($Q_P A_0$) and resonance frequency (f_P) are always lower than the unpackaged amplitude ($Q_U A_0$) and resonance frequency (f_U), respectively.

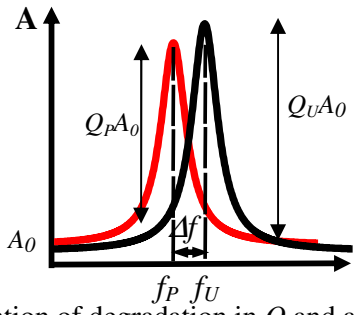


Figure 4.26. Conceptual demonstration of degradation in Q and amplitude after packaging.

In average, the fundamental resonant frequencies of the tested microresonators decreased about 1.3% after packaging. This experiment proves that thermal decomposition of the Unity sacrificial polymer and the packaging process does not alter the device performance significantly. Since the support loss and thermoelastic damping are independent of the surface residues, only the surface loss is considered. Since the modulus of Unity is very different from that of silicon, the residue can increase the surface loss, and so reduce the Q [108].

$$Q_{Surface} = \frac{Wt}{3W + t} \frac{E_{Si}}{2E_{DS}\delta} \tag{4.12}$$

where W is the beam width, t is the beam thickness, E_{Si} is the SCS Young's modulus, δ is the residue thickness (can be measured by AFM) , E_{DS} is a constant related to the surface stress. SEM view of the Unity cavity on top of beam resonators after decomposition is shown in Figure 4.27. Decomposition can leave some residue on the surface and inside the capacitive gap.

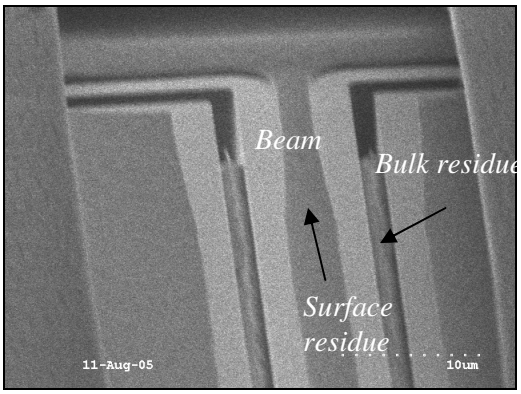


Figure 4.27. View of Unity residues in a non-successful decomposition after removal of cap using RIE.

Figure 4.28 shows the typical images of the surface morphology for Unity residues on silicon substrate, obtained using a Veeco Atomic Force Microscope (AFM) in tapping mode showing an average thickness of δ=19 nm for the residues.

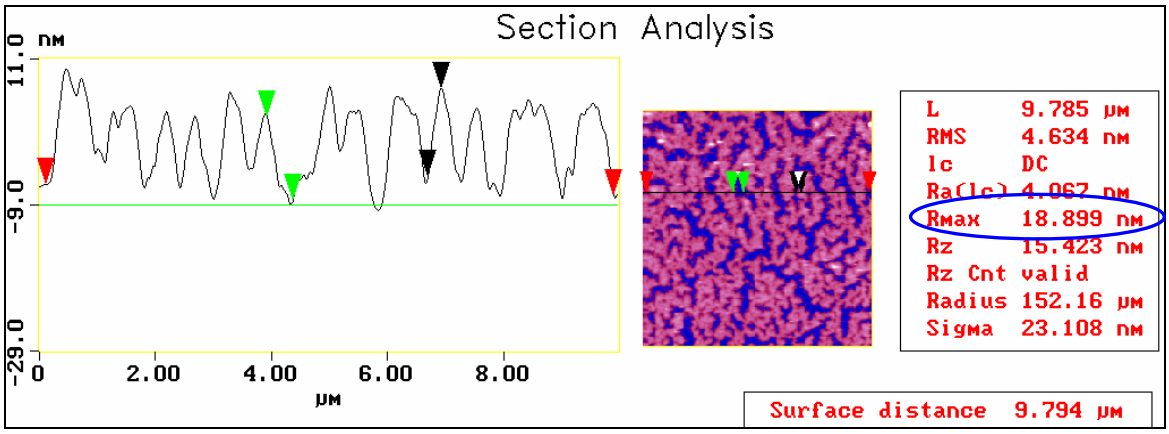
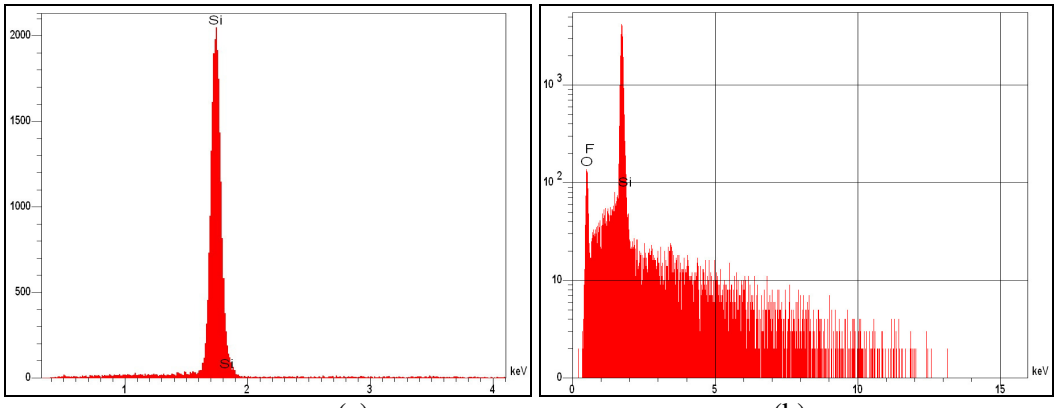


Figure 4.28. AFM inspection of the Unity residue [103].

The other aspect of residue analysis is to study the residue elements, and to know how decomposition temperature changes the remaining elements. An Energy Dispersive X-ray (EDX) Analysis was performed. The emitted X-ray spectra, has peaks, corresponding to the energies of specific elements. Also, the composition percentage can be calculated. Figure 4.29 shows the spectrum of reference silicon and the residues.



(a) (b)

Figure 4.29. a) Spectrum of the pure silicon, b) Spectrum of the residue decomposed at 180°C.

The analysis result is summarized in Table 4.6. It is evident that most of the residue has carbon and fluorine content (from Photo Acid Generator, PAG), as expected [101]. Hydrogen can not be detected since it is below the measurement window. Fluorine is a

by-product of the pentaflourobenzene moieties in the PAG that remain after the decomposition of the PAG [101]. Acid generation using both photolytic (when UV exposed) and thermolytic (when the temperature reaches the decomposition temperature of the PAG) increases the rate of acid generation and fluorine-based byproduct residue.

Table 4.6. EDX analysis of the Unity residues decomposed at 180°C [101]

	Atomic Percentage			
	C	O	F	Si
Elements	**2.52**	**6.65**	**4.51**	**86.31**

4.4. Packaging of HARPSS Varactor

Various types of RF tunable capacitors were fabricated through the self aligned method (Figure 3.4.right) and packaged through the hermetic method explained in Figure 4.7. Figure 4.30 shows a HARPSS RF varactor with 0.8 μm capacitor gap and 2.5 μm tuning gap. The 0.8 μm gap is defined by sacrificial oxide and the 2.5 μm tuning gap by DRIE. Figure 4.30.c shows the same device after encapsulation with 15 μm Avatrel and 1 μm gold. The gold is evaporated on top of Avatrel to create a near-hermetic package.

As shown in Figure 4.30.d, the Avatrel has a 90° profile, which provides isolation of evaporated gold overcoat from the substrate.

The metal-organic package does not change the DC performance of the device, although it can degrade the RF performance. The mentioned metal-organic package adds a small measured loss, as low as 1.4 dB at 1 GHz and 1.5 dB at 5 GHz to the RF MEMS device, as depicted in Figure 4.31.

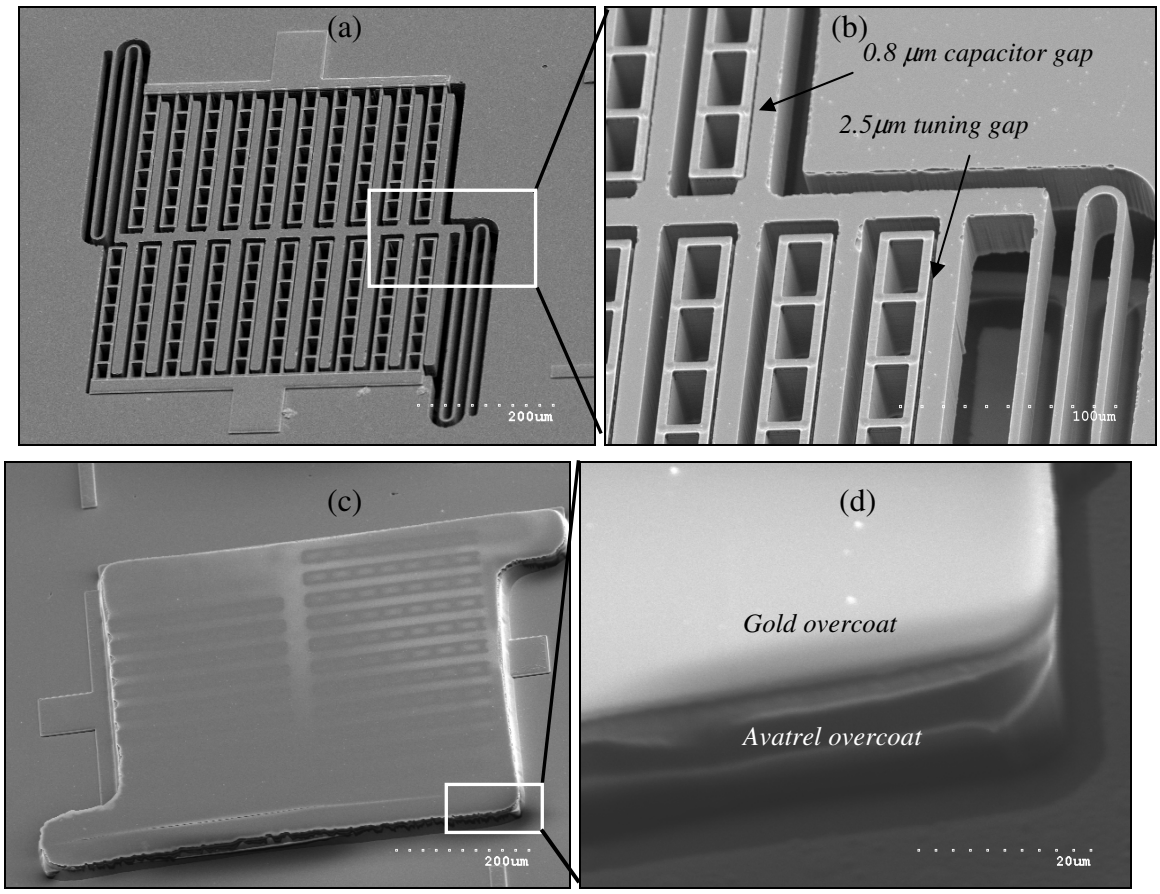


Fig. 4.30. (a) A 60 μm thick HARPSS tunable capacitor: (a, b) Before packaging; (c, d) After packaging using 20 μm thick Avatrel and 1 μm thick gold [103].

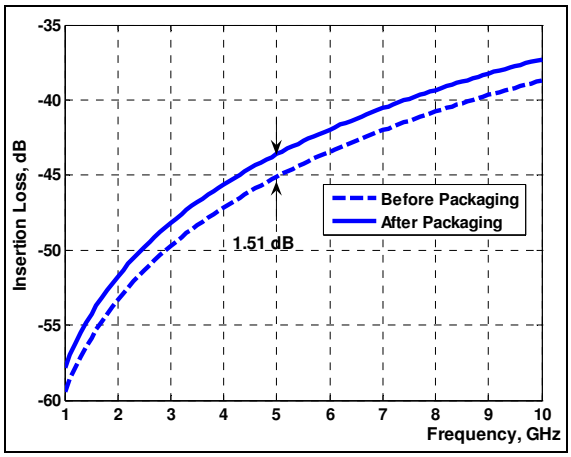
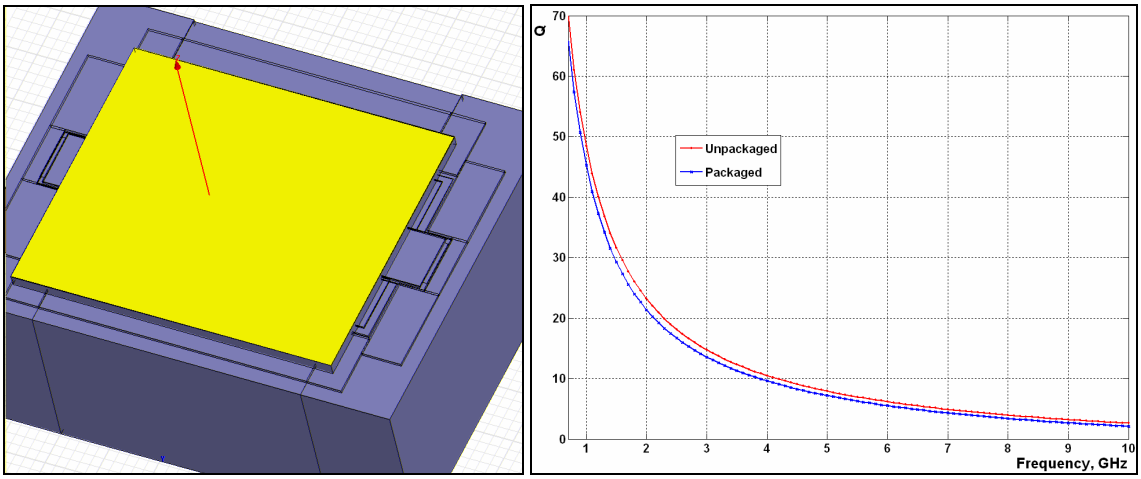


Fig. 4.31. Measured insertion loss of the HARPSS tunable capacitor before and after gold-Avatrel packaging [103].

As can be observed in Figure 4.32, a 1 µm thick/20 µm thick Avatrel/gold package results in degradation of Q from 50 to 45 at 1 GHz.



(a) (b)

Figure 4.32. a) Simulation of the packaged HARPSS varactor in HFSS, b) *Q* factor for the 60 µm thick packaged varactor using 20µm Avatrel and 1 µm gold overcoat.

The reduction in Q is due to increased loss of the package capacitance and has less impact at higher frequencies. The same device can be capped by a bonded glass resulting in lower loss, but the package size will be larger [109]. This is because of the minimum size requirement for the seal ring and the separation between the ring and the device.

4.5. Encapsulation of the HARPSS Accelerometer

A 1.2 mm × 1mm HARPSS accelerometer was encapsulated using the PVD method to evaluate the PVD method for big and complicated MEMS structures. The single-sided static sensitivity of the accelerometer after packaging is measured to be 0.27 pF/g and the estimated Mechanical Equivalent Noise Acceleration (*MNEA*) is 5.0 µg/√Hz, as shown in Figure 4.33. Table 4.7 is a summary of the measured performance for the 50 µm thick HARPSS accelerometer with 1 µm air gap, packaged via PVD scheme [100].

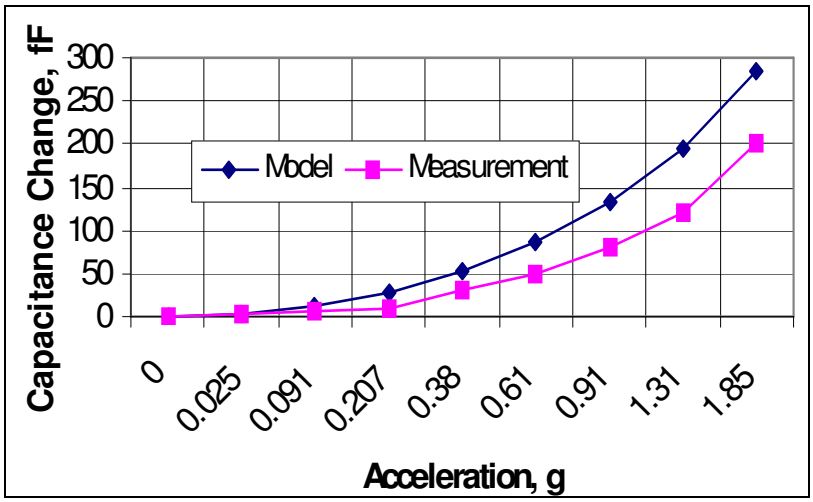


Figure 4.33. Electrostatic sensitivity testing of packaged silicon accelerometer with PVD method [100].

Table 4.7. Measured parameters of the packaged HARPSS Accelerometer

Mechanical parameter			**Physical parameter**		
M (Kg)	f_0 *(Hz)*	*K (N/m)*	C_0 *(pF)*	*S (pF/g)*	*MNEA (μg/√Hz)*
0.3×10^{-6}	1970	46	2.12	0.271	5.0

Figure 4.34 shows the packaging profile. After dispensing Unity and patterning 120 μm thick Avatrel, the decomposition was performed at 250°C for two hours. The close-up view of the poly-Si electrodes and SCS movable mass is magnified in Figure 4.34.c and 4.3.4.d after breaking the polymer cap. The sensor has a non-corrugated electrode structure. It is notable that any reside inside the gap in a 0.36 mm^2 area can stop the sensor from deflection, proving a successful decomposition of Unity with minimum amount of residues. The rest capacitance did not change after packaging. Therefore, the CTE mismatch between Unity and silicon did not create any electrode deformation and change in the gap size during decomposition.

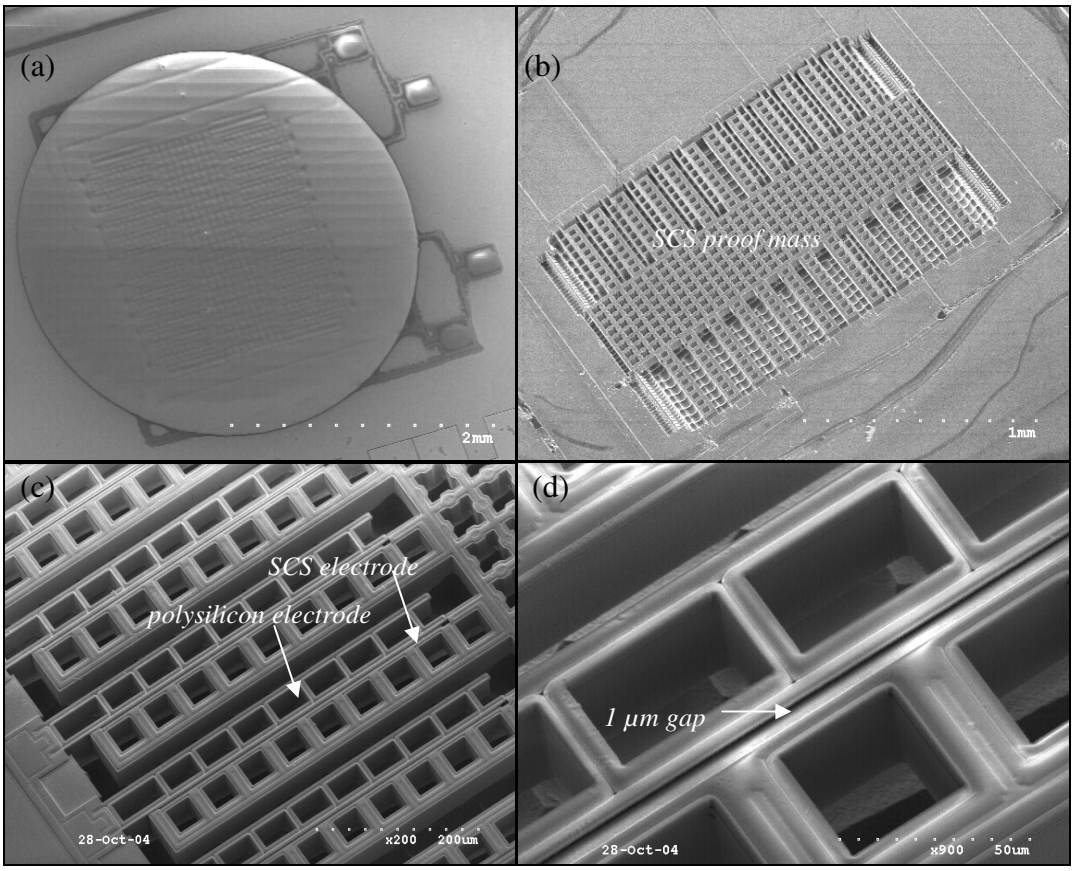


Figure 4.34. (a) Packaged HARPPS accelerometer after PVD, (b) Same accelerometer after breaking the cap, (c) Close up view of the electrode area [99].

Shown in Figure 4.35 shows the uniform and repeatable patterns of 4 mm wide Unity, dispensed using a syringe on a 4" wafer. Same method was used to encapsulate the accelerometers.

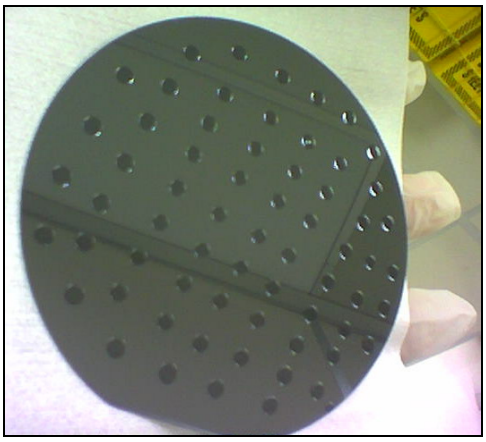
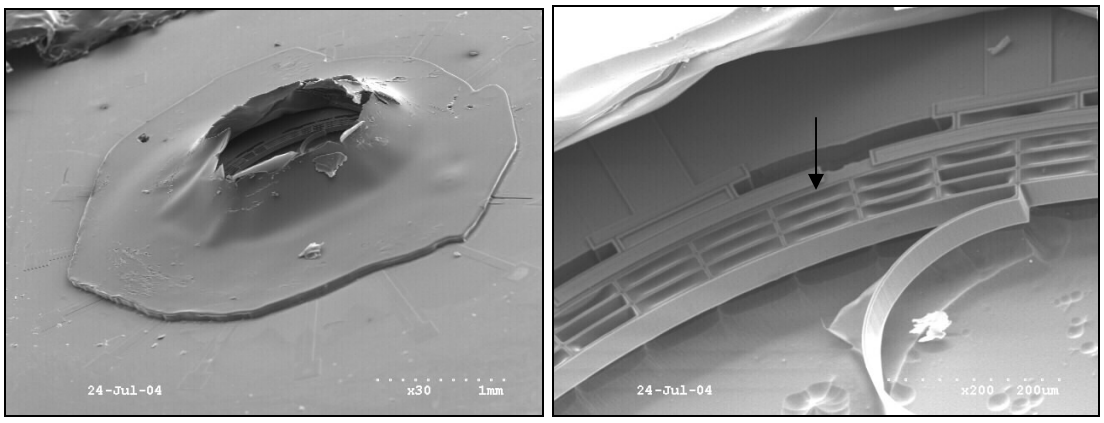


Fig.4.35. Sacrificial material patterns across a 4" wafer by dispensing (PVD).

4.6. Encapsulation of HARPSS Ring Gyroscopes

In order to evaluate the PVD method on gyroscopes, a 2 mm wide, 50 µm thick polysilicon HARPSS ring gyroscope with 1 µm gap spacing and 200 µm deep cavity was fabricated. Unity was dispensed using a 1 mm in diameter syringe, covered with 120 µm Avatrel, and decomposed in oven at 180°C for one and half hour. Figure 4.36.a shows the packaged gyroscope after opening a window in the Avatrel cap. Figure 4.36.b shows the close up view of the electrodes, residues of Unity can be easily observed inside and on top of the polysilicon rings. This means that the decomposition temperature-time was not enough to completely remove a 200 µm thick Unity in a 3 mm^2 area. Experiments on different-size Unity features show that large Unity patterns decompose slower than small patterns. Also thick Unity patterns require longer decomposition time than thin patterns.



(a) (b)

Figure 4.36. (a) Packaged gyroscope using PVD, b) Close up view of electrodes and ring.

At higher temperature, the thermal decomposition of the polymer and PAG into small, volatile products is more efficient. Another attempt using a decomposition temperature of 260°C was done for a 1mm wide ring gyroscope. Figure 4.37.a shows the gyroscope after release step and prior to packaging. Figure 4.37.b is the same device after

dispensing Unity to cover the ring and the electrodes. Figure 4.37.c is the device after decomposing the Unity. Figure 4.37.d is the view after removing the cap. The electrodes are shown in Figure 4.37.e and 4.37.f, confirming a very clean cavity and intact device structure. In addition to the cap, standard off-the-shelf plastic or ceramic packages with lead frames can be utilized for the final assembly of the packaged gyroscope.

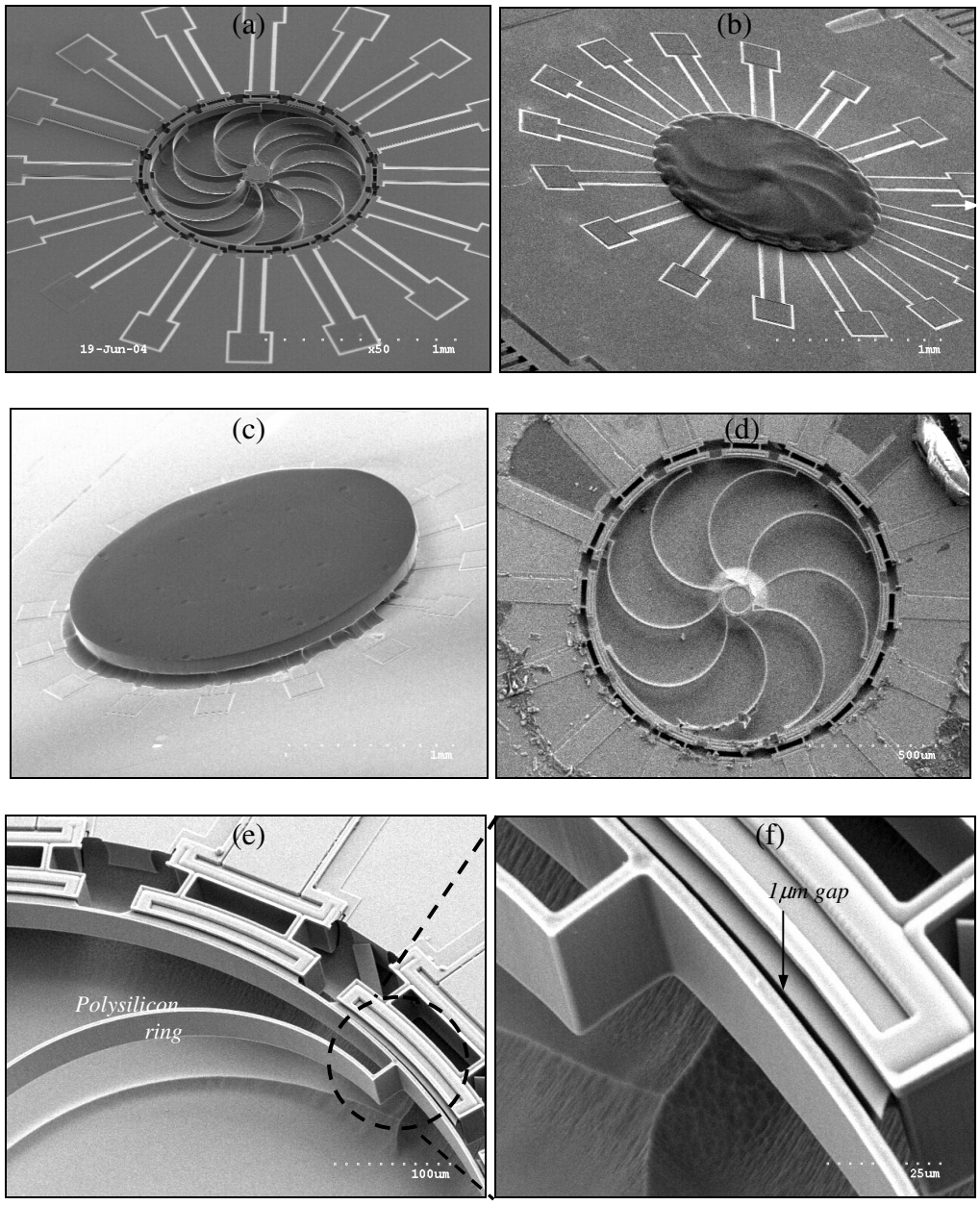


Figure 4.37. Fabricated polysilicon ring gyroscope; a) Before packaging. b) After dispensing. c) After PVD. d) After breaking the cap. e), f) close-up views [99].

CHAPTER V

CONCLUSION AND FUTURE DIRECTIONS

The focus of this dissertation is on development and characterization of a new low-cost, CMOS compatible wafer-level hermetic packaging technology for microelectromechanical systems (MEMS) including the micromachined element and the interface circuit. This technique utilizes decomposition of a sacrificial polymer through an overcoat polymer to create buried cavities on top of resonant/movable parts of the MEMS device, followed by metal coating to provide hermeticity.

The main contributions of this work are to establish a platform for packaging of MEMS by creation of metal-organic capsules on top of the active area using sacrificial embedded cavities. The advantages of this encapsulation approach compared to other MEMS packaging techniques are that it is a low-temperature process that can be used for packaging a wide variety of MEMS including metallic structures, it produces a low-profile encapsulating cover, and can be performed on any substrate. Thermal decomposition of sacrificial polymer is performed through a solid perforation-free capsule, which eliminates the steps needed in some other sacrificial-based techniques to seal a perforated [26, 29] or porous [28] cover. It does not require high temperature deposition and etching of sacrificial materials [15, 26, 28] and is stiction-free. The

overcoat geometry can be scaled according to application to tailor different sizes from microscale to millimeter-scale. The polymer packaging does not require wafer-to-cap alignment and bonding. This method provides small interconnects, which is critical for the RF MEMS devices. Moreover, very complicated structures that need access to multiple pads in the periphery and center (e.g. tuning fork gyroscopes) can be packaged, a feature that is not available with wafer-bonding. This approach is applicable to both surface and bulk micromachined devices.

Other methods for formation of dry-released air-gaps include dry release of dendritic sacrificial material to fabricate cantilever beams [110], depolymerization of polyoxymethylene deposited by hot-filament CVD [111], or polycarbonates to fabricate nanofluidic devices by electron beam lithography [112]. Compared to those methods, our sacrificial polymer can be applied using low-cost tools including spinners or syringe.

For MEMS that need semi-hermetic packaging, standard IC assembly processes can be used. This requires physical protection of MEMS prior to assembly, which is possible through low-cost polymer encapsulation techniques. This includes creation of embedded cavity on top of the active MEMS using sacrificial polymer by either spin casting or dispensing the sacrificial polymer. Then the overcoat polymer with appropriate thickness will be photo-defined, followed by decomposition to create the embedded air or vacuum cavity. The permeability evaluation of the Avatrel overcoat and hermeticity analysis of the vacuum packaged resonators have been performed on a large number of resonators by using different cap thicknesses and temperatures. Some of resonators were tested one month after polymer encapsulation and no change was observed compared to resonators that were tested right after encapsulation. Thermal cycling of the metal-organic cap

shows that chromium is a suitable thin-film metal to be used in this method. For metal films thicker than a few microns, metal electroplating should be used instead of DC sputtering to reduce the residual stress.

To evaluate the packaging, we demonstrate that the DC and RF key performance metrics of the packaged devices (e.g. mechanical Q factor and resonance frequency of the resonator, electrical Q factor of the varactor, and static sensitivity of the accelerometer) do not degrade considerably after packaging. This proves two important aspects of the packaging technology: 1) Low-temperature decomposition of Unity can form a clean air/vacuum cavity without leaving any residues inside the transduction gap, causing considerable deformation in the overcoat or adding any stress in the MEMS device. A critical attribute of the temperature for forming the air-gap is that the electrical and mechanical structures are not distorted during packaging. 2) The thick dielectric polymer is low-loss, enabling a wideband packaging required for RF and microwave components including micromachined passives and switches. In addition to package characterization, the polymer permeability, and the yield of the packaging process have been evaluated.

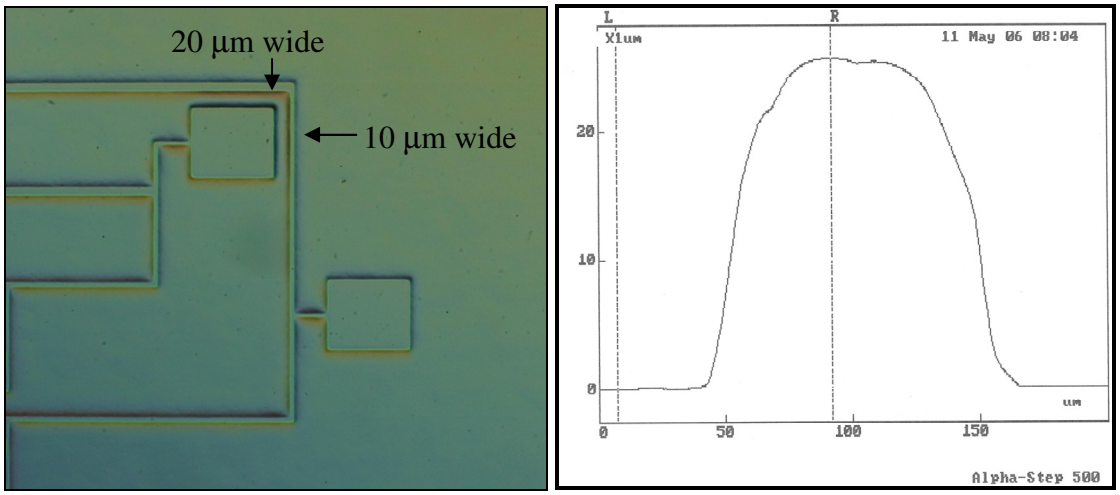
Future directions include reliability testing of the vacuum packaged resonators and hermetically packaged RF varactors, and accelerometers. The hermeticity evaluation includes comparing the Q of a high-Q resonator before and after packaging, and monitoring Q, or the maximum cap bending at center (Z_{max}) for a long period of time. Evaluation of the metal-organic package reliability includes fast and slow thermal cycling, shock analysis, and also survivability test under plastic molding conditions. One of goals for organic encapsulation is protecting the MEMS at the wafer-level prior to plastic or ceramic molding. The plastic molding is performed at temperatures as high as

175°C and pressures as high as 1000 psi (70 atm) [102, 113]. To investigate the survivability of the packaged samples in a real molding environment, it has to be verified whether the elevated temperature and pressure can damage the package or create cracks or make significant deflection in the microshell.

Appendix A. Packaging Process Details

This appendix covers the summary of the patterning and etching steps for the packaging.

1. **Unity 200P patterning, target thickness=9 μm**
    a. Spin coat at 500 rpm/100 rpm/sec/5 sec + 3800 rpm/500 rpm/sec/40 sec
    b. Soft-bake on hotplate at 110 C for 10 minutes.
    c. Deep UV exposure, 1 J/cm^2 in Suss MJB3
    d. Dry develop on hotplate at 110 C for 6 to 10 minutes
    e. Rinse in isopropanol for about 10-15 seconds
    f. Dry with nitrogen gun
    g. RIE Descum in 200 W oxygen plasma

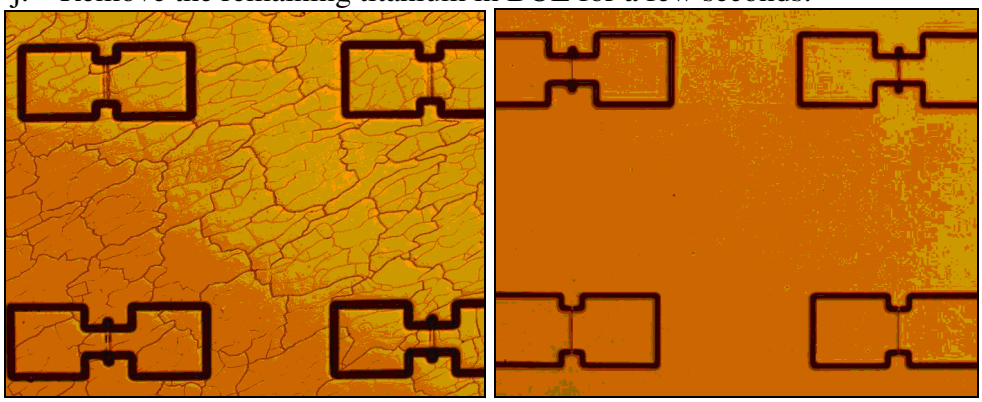


(a) (b)

Figure A.1. a) 10 μm and 20 μm wide traces by photo-patterning Unity, b) Thickness measurement of Unity spun coated at 1500 rpm using Alpha Step contact profiler shows very smooth sidewalls.

2. **Unity etching, target thickness=10 μm**
    a. Spin coat at 500 rpm/100 rpm/sec/5 sec + 3800 rpm/500 rpm/sec/40 sec
    b. Soft-bake on hotplate at 110°C for 10 minutes.
    c. Evaporate 400 °A titanium at 0.5 °A/sec
    d. Spin coat SC1827 at 2000 rpm/300 rpm/sec/30 sec
    e. Soft bake at 85°C for 2 minutes
    f. H-line (405 nm) expose at 200 mJ/cm^2 in Suss MA6 aligner
    g. Develop in MF-319 for 1-2 minutes
    h. Etch titanium in BOE for about one minute.

i. RIE 400W oxygen plasma for about 5-6 minutes or until Unity is gone.
j. Remove the remaining titanium in BOE for a few seconds.



(a) (b)

Figure A.2 View of resonators right after Unity coating and 500A° titanium sputtering, b) after Unity coating and 500 A° titanium evaporation.

3. Buffer oxide deposition

a. Open the Plasmatherm RIE chamber and set the standby temperature to 100°C
b. After the temperature is reached, place the sample after patterning Unity and start depositing PECVD oxide at 100°C with the following parameters:
Pressure: 600-700mT
Platen power: 35W
Chemistry: 200 sccm SiH_4, 450 sccm N_2O

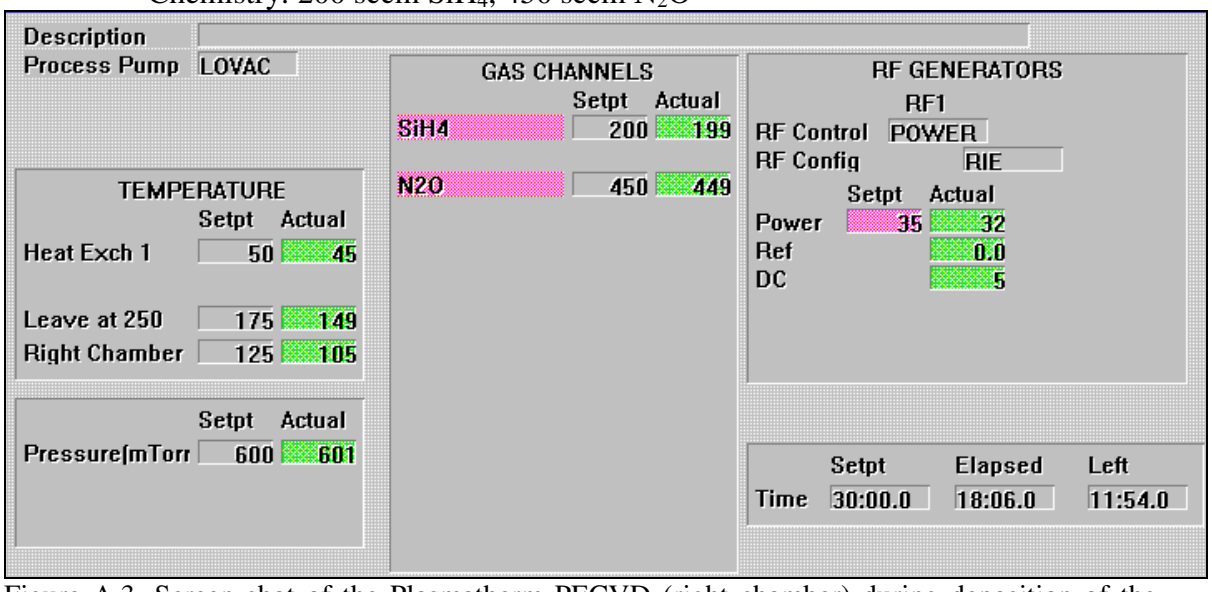


Figure A.3. Screen shot of the Plasmatherm PECVD (right chamber) during deposition of the glass. The PECVD Oxide film is slightly compressive.

Deposition of thick glass on Unity can cause decomposition and cracking of Unity. For depositing a thicker layer of glass, Spin on Glass (Honeywell 512B) can be spin coated on Unity and cured.

4. **Avatrel 2000P Patterning, target thickness=10 μm**
    a. Spin coat at 500 rpm/100 rpm/sec/5 sec + 4000 rpm/500 rpm/sec/60 sec
    b. Soft-bake on hotplate at 110°C for 15 minutes.
    c. I-line (365 nm) exposure, 250 mJ/cm^2 in Suss MA-6 aligner
    d. Post-exposure bake in an oven at 110°C for 15 minutes
    e. Spray develop using Bioact developer for one minute
    f. Rinse in isopropanol for about a minute
    g. Descum in 400 W oxygen plasma for half a minute

5. **Unity decomposition**
    a. Ramp 5°C/min up to 150°C, dwell for half an hour in Lindberg furnace
    b. For RF MEMS, ramp 1°C/min up to 220°C, dwell for two hours
    c. For resonators, ramp 1°C/min up to 280°C, dwell for one and half hours

Table A.1. Summary of polymer packaging process

Parameter	Unity (9μm)	Avatrel (10μm)
Spin coating speed	3800rpm	4200rpm
Soft bake	10min/110°C	10min/100°C
Exposure	1J/cm^2 (240nm)	0.25J/cm^2 (365nm)
Post-exposure bake	-	10min/100°C
Development	~10min/110°C	Spray ~1min
Decomposition	1°C/min to 160°C, hold for 1 hour 1°C/min to 250°C, hold for 2 hours	

6. **Metal deposition and etching**
    a. Pre-cure the Avatrel polymer inside CVC DC sputterer up to 150°C
    b. Start deposition of the seed layer:
        chromium or titanium at 7% power in a pressure of 20 mT (station 3 or 4)
    c. Start deposition of the structural layer:
        chromium at 7% power in a pressure of 6 mT (station 3 or 4)
        or
        aluminum at 15% power in a pressure of 6 mT(station 1)
        or
        gold at 15% power in a pressure of 6 mT (station 3 or 4)
        or
        copper at 15% power in a pressure of 6 mT (station 2)
    d. Spin coat HMDS at 2500 rpm/500 rpm/sec/15 sec
    e. Soft-bake on hotplate at 110°C for 1/2 minutes.
    f. Spin coat SC1827 or MF319 at 2500 rpm/500 rpm/sec/15 sec
    g. Soft-bake on hotplate at 110°C for 60-90 seconds.
    h. H-line expose at 200-300 mJ/cm^2
    i. Develop in MF-319 for 2-4 minutes
    j. Etch metal in metal etchant (gold/copper) or in RIE (aluminum/chromium/titanium).
    k. Strip photoresist in acetone (do not use the asher since the metal will crack, do not use 1112A for aluminum since it attacks the aluminum)

l. Remove the buffer oxide layer in BOE or RIE using metal as a mask (do not use BOE on aluminum)

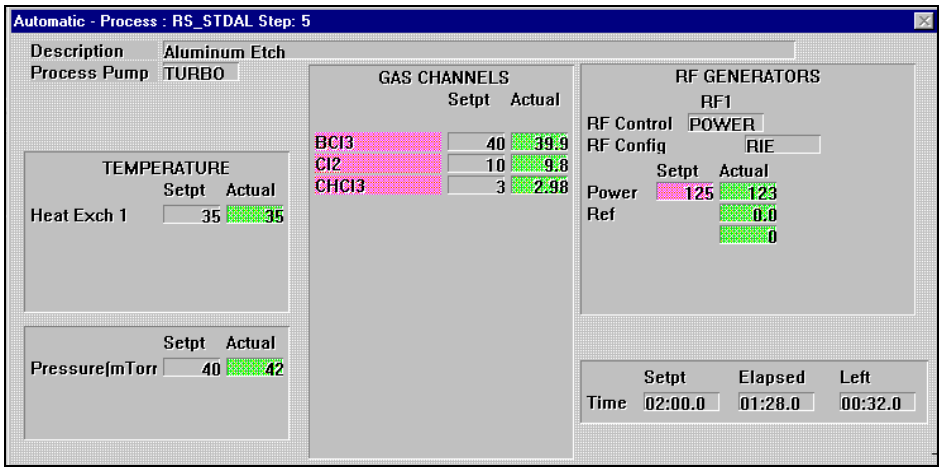


Figure A.4. Screen shot of the Plasmatherm RIE (left chamber) during etching of aluminum.

Appendix B. HARPSS Processing Details for SCS MEMS

This appendix lists HARPSS process steps in detail. Important characterization steps such as electron microscope and optical profilometry of trenches, and also surface roughness of LPCVD polysilicon are shown in Figures B1 through B3.

Step	Description	Parameters
1. Isolation	Clean wafer	TCE, Acetone, Methanol, DI water Piranha (4:1 H_2SO_4, H_2O_2) SC-1 (4:1:1 HCL:H_2O_2:H_2O)
	1 μm low-stress LPCVD nitride deposition in Tystar furnace (Appendix C)	150 mT, 850°C SiH_2Cl_2: 100 sccm, NH_3: 15 sccm, rate: 44°A/min
	Spin/bake HMDS and spin SC1827 photoresist in Suss RC-8 spinner	Cover 1/3 of the wafer with HMDS: 4000rpm, 1000rpm/s, 20 s. Bake HMDS 115°C for 30 s. Cover 2/3 of wafer with 1827: 1000rpm, 1500rpm/s, 5 s. 2000rpm, 500rpm/s, 30 s.
	Soft bake on hotplate	115°C for 1 min
	Exposure in Suss MA-6 aligner	I-line, 200 mJ/cm^2, hard contact, 25μm alignment gap.
	Develop in beaker	MF-319 developer for 1min Dip in DI water for 1min Wash with DI water
	Hard bake on hotplate	5 min at 115°C
	RIE nitride in PlasmaTherm-ICP	Platen power: 100W Coil power: 250W Pressure: 5 mTorr CF_4: 20 sccm rate: 1.05μm/s
	Strip in Gasonics asher	2 min

Step	Description	Parameters
2. Trench Definition	Spin/bake HMDS and spin SC18127 photoresist in Suss RC-8 spinner	Cover 1/3 of the wafer with HMDS: 4000rpm, 1000rpm/s, 20 s. Bake HMDS 115°C for 30 s. Cover 2/3 of wafer with 1827: 1000 rpm, 1500 rpm/s, 5 s. 2000 rpm, 500 rpm/s, 30 s.
	Soft bake on hotplate	115°C for 1 min
	Exposure in Suss MA-6 aligner	I-line, 200 mJ/cm^2, hard contact, 25 µm alignment gap.
	Develop in beaker	MF-319 developer for 1min Dip in DI water for 1min Wash with DI water
	Hard bake on hotplate	5 min at 115°C
	DRIE silicon in STS-ICP (5 ms pulse width, 25% duty cycle)	Platen power/freq: 15W/13.56MHz Coil power/freq: 700W/13.56MHz Pressure: 15 mTorr SF_6/O_2: 130/13 sccm, 10 s C_4F_8: 100 sccm, 8 s rate: 1.5µm/s
	Strip in Gasonics asher	2 min

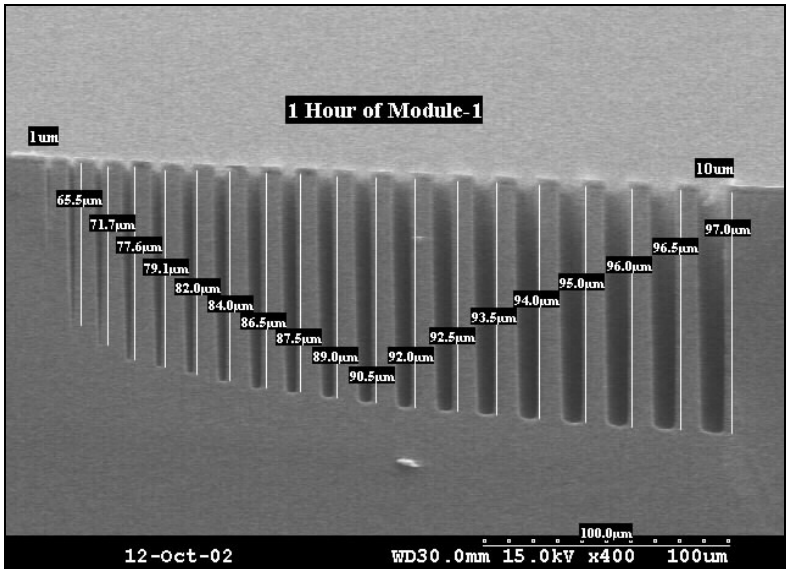


Figure B.1.Cross section of trenches after 1 hour DRIE in STS-ICP.

Step	Description	Parameters
3. Trench Refill	Pre-furnace clean	TCE, Acetone, Methanol, DI water Piranha (4:1 H_2SO_4, H_2O_2) SC-1 (4:1:1 HCL:H_2O_2:H_2O)
	0.5-2 µm thermal oxide growth in Tystar furnace	850°C O_2: 1000 sccm, H_2/O_2: 185 sccm,
	Oxide boron doping in Tystar furnace	1 hr 1050°C O_2: 200 sccm, N_2: 5000 sccm,
	2-4 µm polysilicon deposition in Tystar furnace	588 °C 250 mT SiH_4: 100 sccm,
	Poly-Si boron doping in Tystar furnace	2 hrs 950°C O_2: 200 sccm, N_2: 5000 sccm,
	Poly-Si annealing in Tystar furnace	1 hr 950°C O_2: 200 sccm, N_2: 5000 sccm,
	Remove BSG in BOE	2-4 min

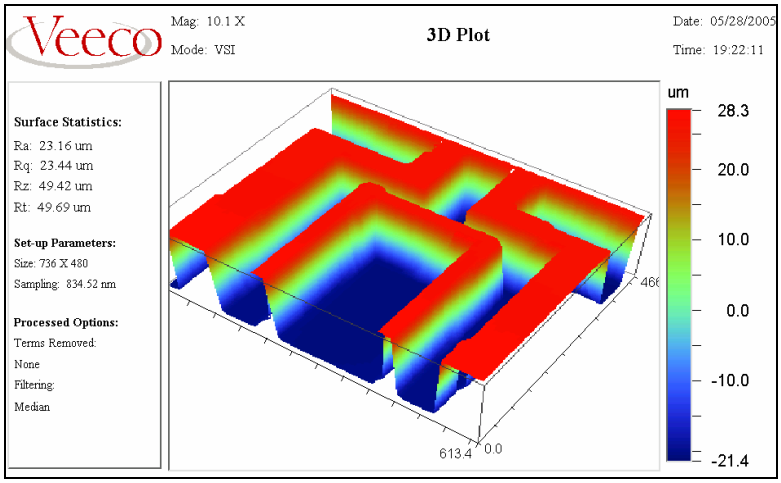


Figure B.2. Optical profilometry for end point detection of polysilicon at the bottom of wide trenches, using a Veeco NT 3100 optical profilometer.

Step	Description	Parameters
4. Polysilicon Isolation	Spin/bake HMDS and Spin Photo-Resist in RC-8	Cover 1/3 of the wafer with HMDS: 4000rpm, 1000rpm/s, 20 s. Bake HMDS 115°C for 30 s. Cover 2/3 of wafer with 1827: 1000 rpm, 1500 rpm/s, 5 s. 2000 rpm, 500 rpm/s, 30 s.
	Soft bake on hotplate	115°C for 1 min
	Exposure in Suss MA-6 aligner	I-line, 200 mJ/cm^2, hard contact, 25 µm alignment gap.
	Develop in beaker	MF-319 developer for 1min Dip in DI water for 1min Wash with DI water
	Hard bake on hotplate	5 min at 115°C
	Spin/bake HMDS and spin SC1827 photoresist in Suss RC-8 spinner	Cover 1/3 of the wafer with HMDS: 4000rpm, 1000rpm/s, 20 s. Bake HMDS 115°C for 30 s. Cover 2/3 of wafer with 1827: 1000 rpm, 1500 rpm/s, 5 s. 2000 rpm, 500 rpm/s, 30 s.
	Soft bake on hotplate	115°C for 1 min
	DRIE silicon in STS-ICP (5 ms pulse width, 25% duty cycle)	Platen power/freq: 10W/13.56MHz Coil power/freq: 600W/13.56MHz Pressure: 20 mT SF_6/O_2: 130/13 sccm, 10 s C_4F_8: 100 sccm, 8 s
		Platen power/f: 10→15W/380 kHz Coil power/freq: 600W/13.56MHz Pressure: 30 mT SF_6/O_2: 130/13 sccm, 12 s C_4F_8: 100 sccm, 8 s
		Platen power/f: 15→30W/380kHz Coil power/freq: 700W/13.56MHz Pressure ramped: 30mT→15 mT SF_6/O_2: 130/13 sccm, 10 s C_4F_8: 100 sccm, 8 s
	Strip in Gasonics asher	4 min

5. Release	Spin/bake HMDS and spin SC1827 photoresist in Suss RC-8 spinner	Cover 1/3 of the wafer with HMDS: 4000rpm, 1000rpm/s, 20 s. Bake HMDS 115°C for 30 s. Cover 2/3 of wafer with 1827: 1000 rpm, 1500 rpm/s, 5 s. 2000 rpm, 500 rpm/s, 30 s.
	Soft bake on hotplate	115°C for 1 min
	Exposure in Suss MA-6 aligner	I-line, 200 mJ/cm^2, hard contact, 25 µm alignment gap.
	Develop in beaker	MF-319 developer for 1min Dip in DI water for 1min Wash with DI water
	Hard bake on hotplate	5 min at 115°C
	Release silicon in STS-ICP (5 ms pulse width, 25% duty cycle)	Platen power/freq: 15W/13.56MHz Coil power/freq: 700W/13.56MHz Pressure: 15 mTorr SF_6/O_2: 130/13 sccm (10 s) C_4F_8: 100 sccm (8 sec) rate:1.5µm/s
	Release oxide in HF	HF: DI 1:1 use a tripod Methanol 1hr in Super critical dryer

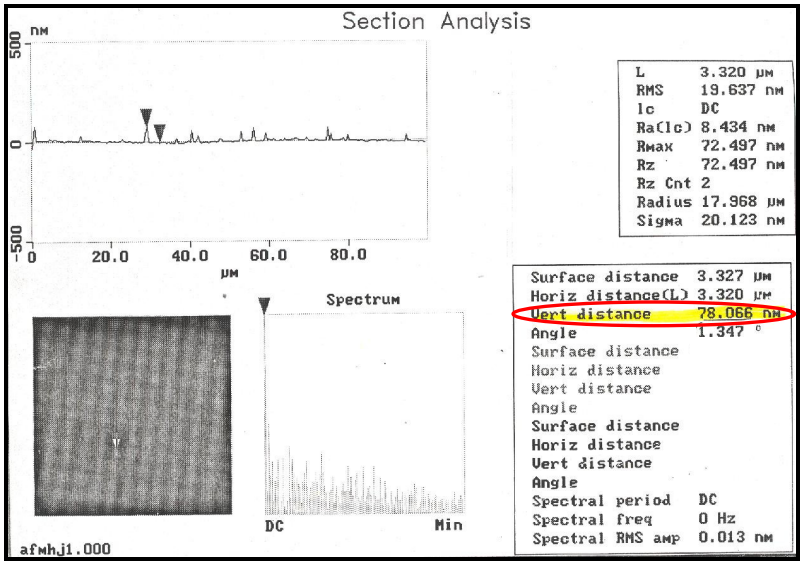


Figure B.3. Roughness measurement of 3 µm thick LPCVD polysilicon using a Veeco AFM in contact mode; the average roughness is about 80 nm.

Appendix C. Details of Low-Stress LPCVD Nitride Process

This appendix covers the characterization of the low-stress LPCVD nitride recipe.

Deposition rate measurement: The deposition rate was measured using a nanospec spectrophotometer to be about 2600-2650°A/hr.

Stress measurement: The stress measurement was done on a full size of 4" wafer perpendicular to the flat. Two measurements, pre-stress scan and post-stressed scan, was done to measure and save the wafer curvature prior to coating. After coating 0.8 µm nitride (deposition time: 3 hours), the wafer was scanned with the same recipe again. The film stress can be calculated from the two data sets to be 74.9 MPa (tensile).

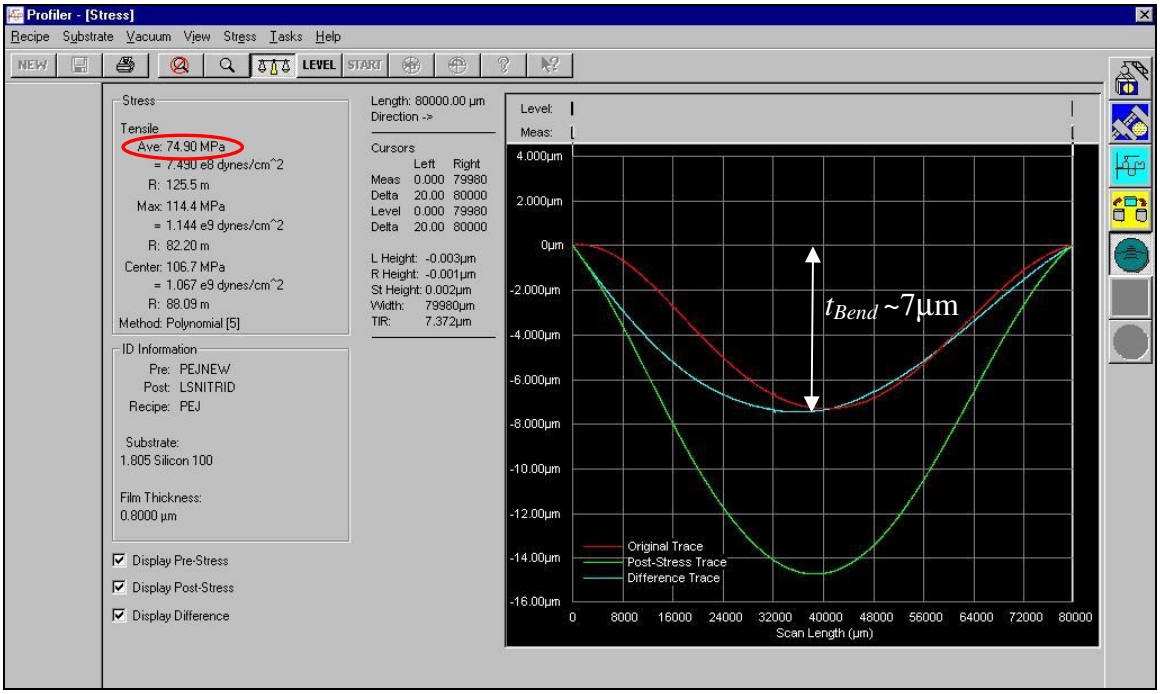


Fig.C.1. Stress measurement using a KLA-Tencor profiler for a 0.8 µm thick low-stress nitride film.

Stress can be calculated using Stoney formula as described by Equation (C.1) [106]:

$$\sigma = \frac{E_{Substrate} H_{Substrate}^2}{6t_{Film}(1-\upsilon_{Substrate})R} \quad \text{(C.1)}$$

The radius of curvature, R, is defined in (C.2) in terms of scan length (W_{Scan}) and deflection (t_{bend}):

$$R = \frac{W_{Scan}^2}{8t_{Bend}} - \frac{t_{Bend}}{2} \quad \text{(C.2)}$$

Changing the deposition parameters, especially the gas ratio will change the film stress, a value of 300 MPa was obtained previously for the low-stress LPCVD nitride film with different parameters in [95].

The process parameters, measured stress and measured phase velocity index of refraction are summarized in Table C.1.

Table C.1. Process parameters of the silicon-rich and stoichiometric LPCVD nitride.

Process	**Temperature, °C**	**$Si_2H_2Cl_2$ flow, sccm**	**NH_3 flow, sccm**	**Pressure, mTorr**	**Measured stress, MPa**	**Measured refractive index**
Low-stress	850	100	15	150	75	2.3
High-stress	800	150	30	300	300	2.0

Modulus measurement: The modulus measurement was performed using a Hysitron triboindenter nanomechanical system, as shown in Figure C.3. Using a diamond tip, a force is applied to the sample in the Z-axis and the deflection of the internal spring is measured. The contact area and contact depth (h_c) are related by a fifth order polynomial in the form of equation (C.3) [114].

$$A = C_0 h_c^2 + C_1 h_c + C_2 h_c^{\frac{1}{2}} + C_3 h_c^{\frac{1}{4}} + C_4 h_c^{\frac{1}{8}} + C_5 h_c^{\frac{1}{16}} \quad \text{(C.3)}$$

The coefficients are dependent on the tip geometry. Knowing the deflection-force curve and contact area, the reduced modulus (E_r) is calculated from equation (C.4).

$$K = \frac{dF}{dh} = 2E_r\sqrt{\frac{A}{\pi}} \tag{C.4}$$

As shown in Figure C.2, data analysis gives E_r=292 GPa.

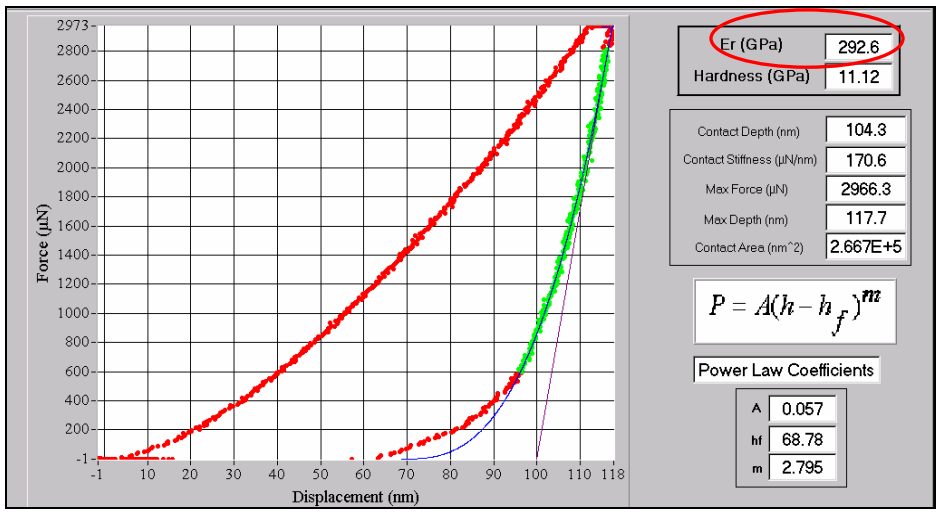


Fig.C.2. Modulus measurement using Hysitron triboindenter for low-stress nitride film.

Etch rate in HF: The etch rate in pure HF is around 18-19 nm/min.

Pinhole characterization: 400 nm low-σ nitride was coated on 1 µm thermal oxide and then put in HF, no visible change was observed in the middle of wafer after 15 min.

Uniformity characterization: Four wafers were deposited with 400nm nitride and uniformity was excellent, as shown in Figure C.3. It was observed that the uniformity improves by increasing the number of wafers.

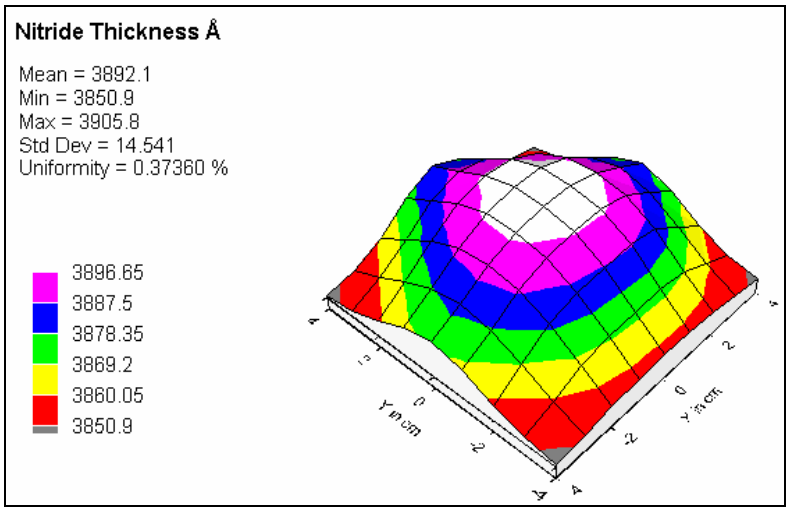


Fig.C.3. Uniformity measurement of a 400 nm thick low-stress nitride over a 4" wafer, using a Wollam ellipsometer.

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